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M. Krneta, I.M. Piatak

Peter the Great St. Petersburg Polytechnic University, St. Petersburg, Russian Federation

LINEARIZATION OF THE ANALOG-TO-DIGITAL CONVERTER FOR AN FPGA-BASED DIRECT DIGITAL RECEIVER

The goal of this work is to provide linearization of the analog-to-digital converter for an FPGA-based Direct Digital Receiver. One of the techniques for implementing that is the LUT-based calibration and correction technique inside the FPGA, which was used for obtaining better characteristics of SNDR, SFDR and INL of the FPGA-based parametrized 14-bit model of pipelined ADC. The experimental part consists of the implementation of the FPGA-based parametrized 14-bit model pipelined ADC using MATLAB/Simulink. Its calibration and LUT-based correction were performed using both MATLAB/Simulink and FPGA. The DDS generator was implemented inside the FPGA. Code was written in Verilog HDL. The values of the dynamic characteristics of the ADC (SNDR and SFDR) were obtained before and after calibration, and compared. The influence of the DC gain and that of the capacitors of the MDAC was taken into account and observed. The influence of changes in the DC gain and capacitor mismatch of MDAC inside the stage was also taken into account for both SNDR and SFDR, as well as for the static characteristic, INL, which was also observed.

Keywords: pipelined ADC, digital error calibration and correction, MATLAB, SFDR, FPGA.

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РАЗРАБОТКА ЦИФРОВОЙ КОРРЕКЦИИ ХАРАКТЕРИСТИК АЦП ДЛЯ ПРИЕМНИКА ПРЯМОГО УСИЛЕНИЯ НА ОСНОВЕ ПЛИС

М. Крнета, И.М. Пятак

Санкт-Петербургский политехнический университет Петра Великого,
Санкт-Петербург, Российская Федерация

Описана линеаризация конвейерного аналого-цифрового преобразователя для цифровых приемников прямого преобразования. Использованы цифровая калибровка и коррекция с применением таблицы соответствия, позволившие улучшить динамические характеристики АЦП. Разработана модель конвейерного АЦП разрядностью 14 бит в среде MATLAB с использованием результатов компьютерного моделирования. Рассмотрено влияние разброса номиналов конденсаторов и величин коэффициента усиления по постоянному току ОУ каскада АЦП на динамические характеристики. Для дальнейшего проведения эксперимента как система калибровки и коррекции на основе таблицы соответствия, так и модель АЦП реализованы с использованием ПЛИС. Результаты

эксперимента с высокой точностью совпадают с результатами компьютерного моделирования и свидетельствуют об эффективности предложенной калибровки и коррекции.

Ключевые слова: конвейерный АЦП; цифровая калибровка и коррекция; MATLAB; динамический диапазон; ПЛИС.

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Introduction

The goal of this study is to provide the linearization of an analog-to-digital converter (ADC) for an FPGA-based direct digital receiver. FPGA stands for Field Programmable Gate Array. In [1] there is a clear correspondence between the sensitivity and signal-to-noise and distortion (SNDR) of the ADC, i. e., the more SNDR, the more sensitive the receiver is, because noise floor is lower. Moreover, spurious-free dynamic range (SFDR) is important, because the less harmonics at the ADC output, the less the probability of blocking the desired low signals by these harmonics and less unwanted received components. Therefore, the correction of the ADC characteristics and especially linearization are important for obtaining high characteristics of the receiver (in particular, sensitivity).

In order to perform the linearization of the ADC, at first it is necessary to provide an ADC model which will take into account some well-known nonlinearities, like non-ideal DC gain and mismatch of the multiplying digital-to-analog converter (MDAC) capacitors inside the pipelined ADC stage. In this work the ADC model inside the FPGA is realized by using a direct digital synthesizer (DDS generator). Instead of sine ROM in DDS, we are using ROM with samples from the MATLAB model with nonidealities. So we can introduce nonlinearities in hardware by changing the DC gain and capacitor mismatch in software in the model of the ADC (MATLAB/Simulink), without buying expensive instruments. In this work, the correction of the dynamic characteristics, SNDR and SFDR, of the ADC is performed using histogram calibration [2].

Literature overview

In the literature we can find results obtained by other calibration and correction techniques for the 14-bit pipelined ADC. For example, for the LMS-based technique at the sampling rate of 200 Msps, SNDR after correction equals 69.5 dB, SFDR 88.9 dB [3]. For the redundancy-based technique [4], the sampling frequency 100 MHz, SNDR is 85.89 dB, SFDR 102.8 dB. For the dither-based technique [5], sampling frequency 100 MHz, SNDR equals 76.56 dB. For the PN-sequence-based technique [6], 125 Msps, 3.5-bit stage architecture, SNDR is 80.86 dB, SFDR 102.27 dB. The combined foreground + background technique, described in [7], at 100 Msps and capacitor mismatch of 0.1 % gave SNDR of 76.8 dB, SFDR of 75.7 dB and INL ±1.2 LSB. For the background technique, described in [8], at 100 Msps and input frequency of 21 MHz, SNDR is 73 dB, SFDR 91 dB, INL 1.3 LSB. The charge-sharing background technique [9] at 100 Msps, input frequency 30 MHz, gives SNDR of 73.1 dB, SFDR of 91 dB and INL 1.1/−1.0 LSB.

In this study the look-up table based (LUT-based) correction is used because it is independent from the architecture of the ADC, it is suitable for many different ADCs, it is easy to perform as IP-block for FPGA, it has low power and improves the linearity and accuracy. The disadvantage of this technique is the following: it requires industrial hardware.

Linearization of the ADC

The first task was to implement the parameterized FPGA-based DDS generator. The DDS code was written in Verilog hardware description language (HDL). Memory was initialized inside the FPGA with the external

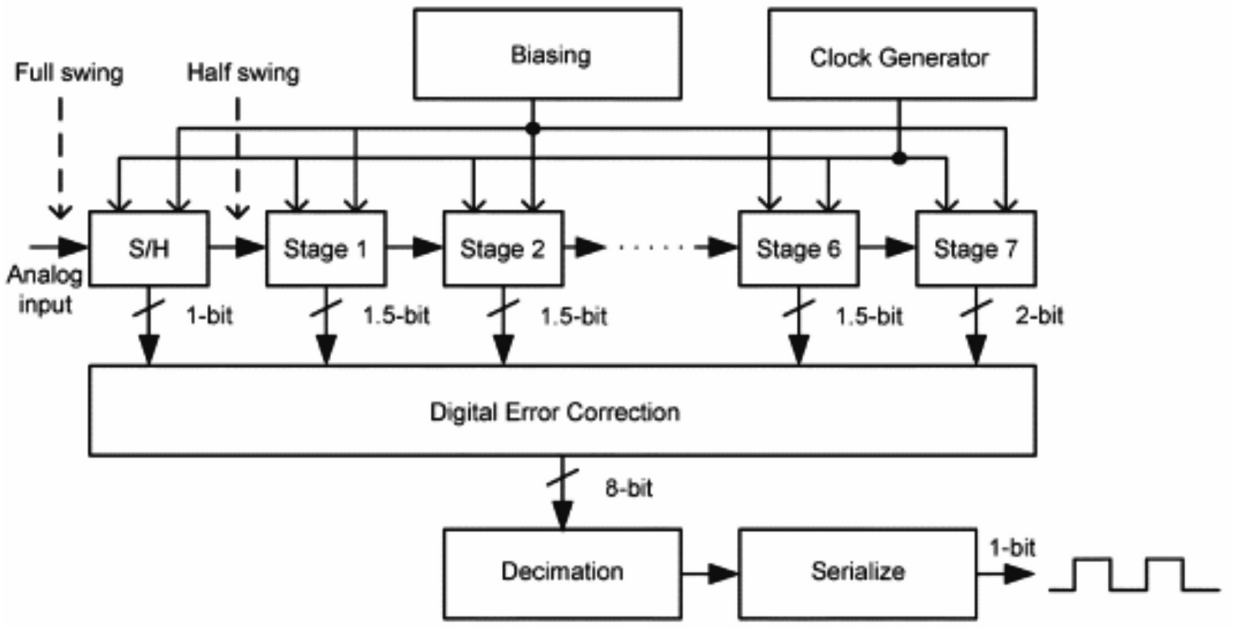

Fig. 1. Structure of the pipelined ADC [11]

file with sine coefficients. The possibility to initialize memory inside the FPGA with external coefficients is a key for building a model ADC and LUT-based correction. The example of the look-up table method is explained in detail in [10].

The Verilog project consists of one module. In this module memory is initialized with an external file, obtained from the non-ideal ADC MATLAB/Simulink model. In this project, hexadecimal sine coefficient values were used. Master clock frequency (MCLK) of the FPGA board has a value of 100 MHz. Sine output was 14 bits long.

Comparing the values from the MATLAB/Simulink ADC model and the values from the output of the DDS, it can be noticed that they are the same, which means that the memory can be initialized inside the FPGA with the external file, containing sine coefficients, and that the DDS generator works, which is exactly what had to be proven.

The next task was the implementation of the parameterized model of the FPGA-based pipelined ADC using MATLAB/Simulink. The structure of the pipelined ADC is shown in Fig. 1.

Fig. 2 shows the MATLAB/Simulink model of the 14-bit pipelined ADC. Its calibration and correction in this part of the study were also done in MATLAB.

The dynamic characteristics SNDR and SFDR of the ADC have been measured. The DC gain of the ideal 14-bit pipelined ADC is 84 dB, the values of the MDAC capacitors C_s and C_f are equal to 1. The sampling frequency equals 100 MHz. Input frequency is 3 MHz.

First of all, the characteristics of the non-calibrated ADC have been obtained. After that, the calibration was done. The SNDR and SFDR values were recorded for the values of the DC gain of 54 and 84 dB. The value of 54 dB is used because it is enough for obtaining good dynamic characteristics using low power op-amps; after the LUT-based correction they are close to ideal values, which will be proven in the next steps. The same procedure was repeated for the fixed DC gain of the ideal 14-bit ADC (84 dB), but in this case the value of the capacitor C_f was changed. The value dC_f was added to the value of the C_f of the ideal 14-bit pipelined ADC (equals 1). The step size of the dC_f is 0.0002, the range of the dC_f values is from 0.001 to 0.002 (change of C_f from 0.1 % to 0.2 %). Those dC_f values are used in order to see the changes of SNDR and SFDR close

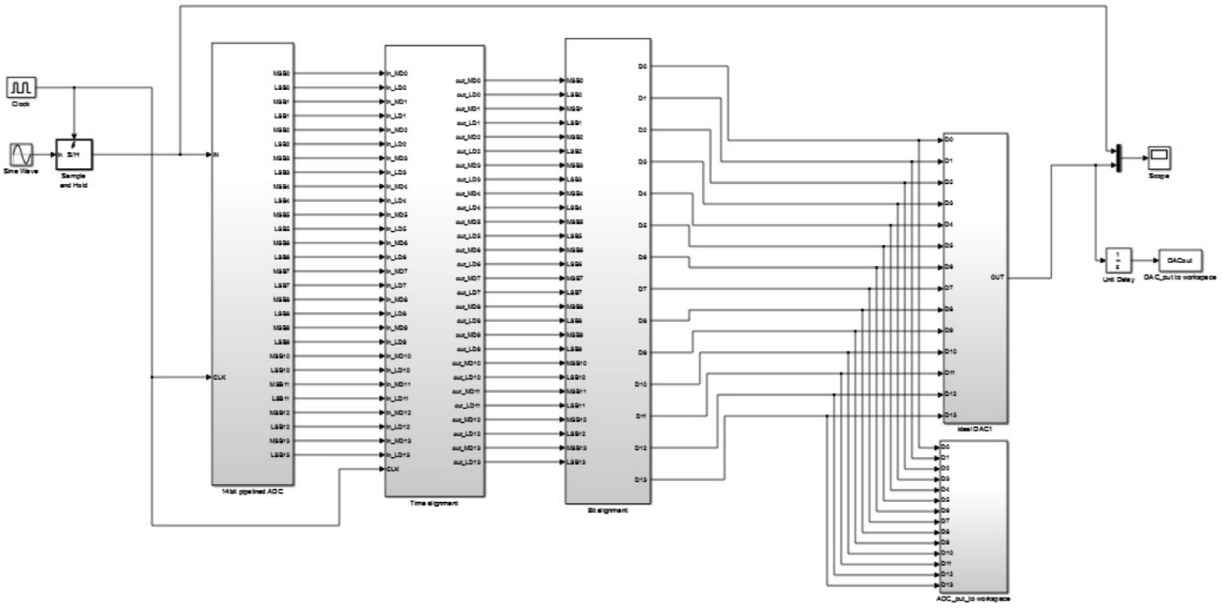

Fig. 2. MATLAB/Simulink model of the 14-bit pipelined ADC

to the down limit of 0.1 %. With this value it is impossible to make a mismatch because of technological operations during manufacturing. After that, the samples from MATLAB are used for initializing the DDS generator memory in the FPGA and after that the sine values obtained at the output of the DDS (Xilinx ISE) are loaded back to MATLAB. They are used in the calibration engine. Table lists the results obtained for the values of DC gain of 84 dB and 54 dB and for the capacitor mismatch of 0 and 0.14 %, before and after correction, using both MATLAB and FPGA. The value of 0.14 % is used as an example between 0.1 and 0.2 %. It can be noticed that the results from MATLAB and FPGA are pretty similar.

The graphs represented in the Fig. 3 and Fig. 4 show the comparison of both characteristics, with MATLAB- and FPGA-obtained values. From their similarity, we can conclude that it is possible to implement the parametrized model of FPGA-based pipelined

MATLAB and FPGA results of SNDR and SFDR for DC gain of 54 and 84 dB and dC_f of 0 and 0.14 %

		dC_f= 0 %		dC_f= 0.14 %	
		84 dB	54 dB	84 dB	54 dB
MATLAB before	SNDR	83.62	57.44	70.84	56.04
	SFDR	87.97	58.12	71.64	56.72
FPGA before	SNDR	83.62	57.44	N/A	N/A
	SFDR	87.97	58.12	N/A	N/A
MATLAB after	SNDR	82.13	77.24	82.03	76.36
	SFDR	90.35	98.76	95.71	97.95
FPGA after	SNDR	82.12	77.21	N/A	N/A
	SFDR	90.28	93.45	N/A	N/A

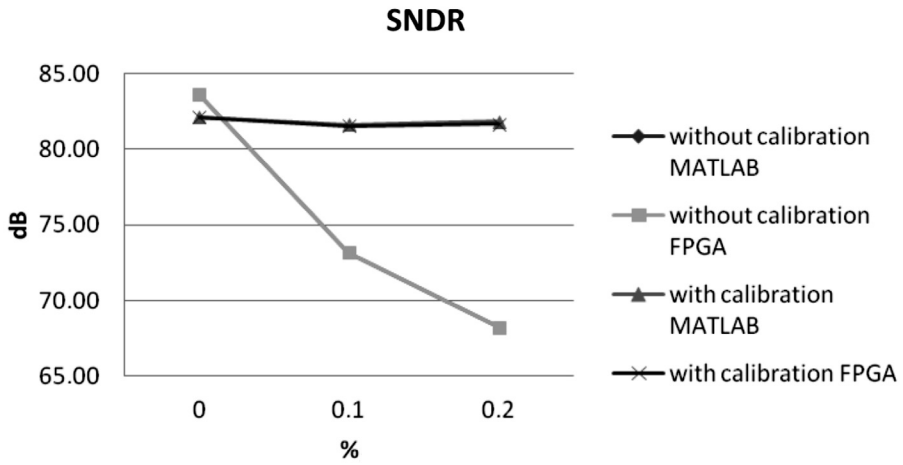

Fig. 3. SNDR characteristic for MATLAB/FPGA values, before and after calibration, DC gain 84 dB

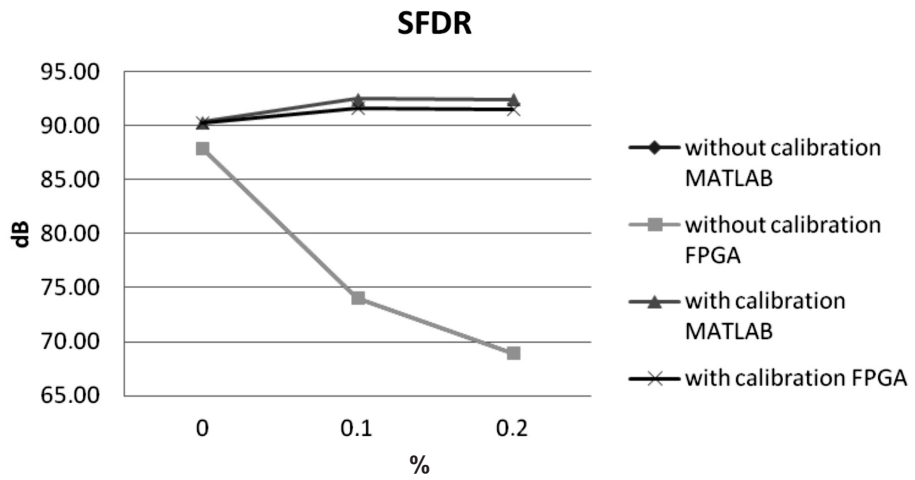

Fig. 4. SFDR characteristic for MATLAB/FPGA values, before and after calibration, DC gain 84 dB

ADC using MATLAB/Simulink.

The results show that the dynamic characteristics of the ADC, SNDR and SFDR depend on the changes of the DC gain, as well as on the changes of the MDAC capacitors. After the calibration, the characteristics became better, i. e., the values of the SNDR and SFDR increased, in comparison with their characteristics before the calibration. In view of this, it can be concluded that the LUT-based calibration improves the dynamic characteristics of the ADC and thus its linearization.

The next step is the implementation of LUT-correction of the parametrized pipelined model ADC, which is done inside the FPGA, using MATLAB. The code was written in Verilog HDL.

The module contains DDS generator and LUT. For both, the memory is initialized with external file, containing sine samples. Samples for LUT are obtained from the LUT of correction in MATLAB/Simulink. Once again, sampling frequency equals 100 MHz. Input frequency is 3 MHz. Again, the dynamic characteristics, SNDR and SFDR, have been observed, as well as the behaviour of the static characteristic INL. The calibration and correction are done for the DC gain of 54 dB and for the capacitor mismatch of 0, 0.1, 0.12, 0.14, 0.16, 0.18 and 0.2 %.

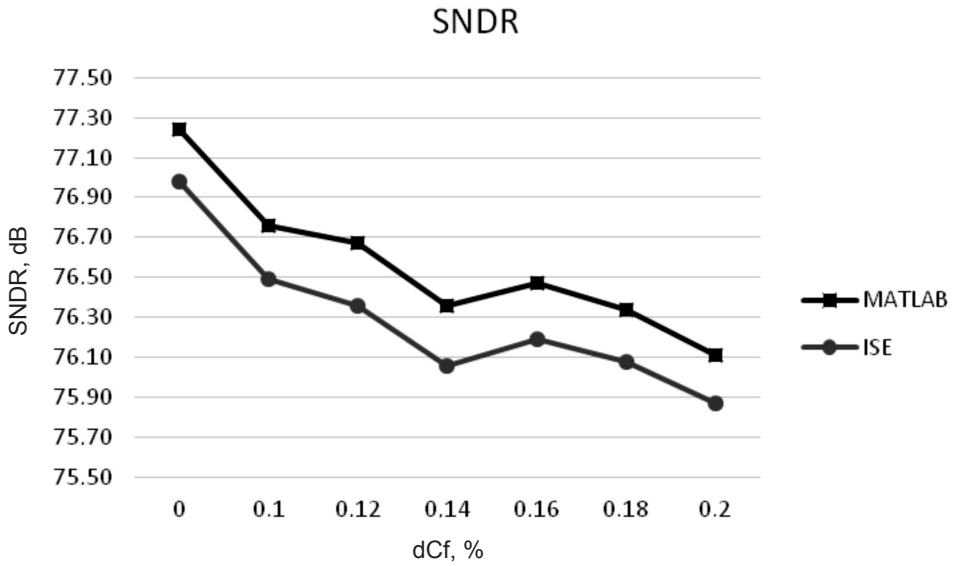

Fig. 5. SNDR after corrections in MATLAB and FPGA

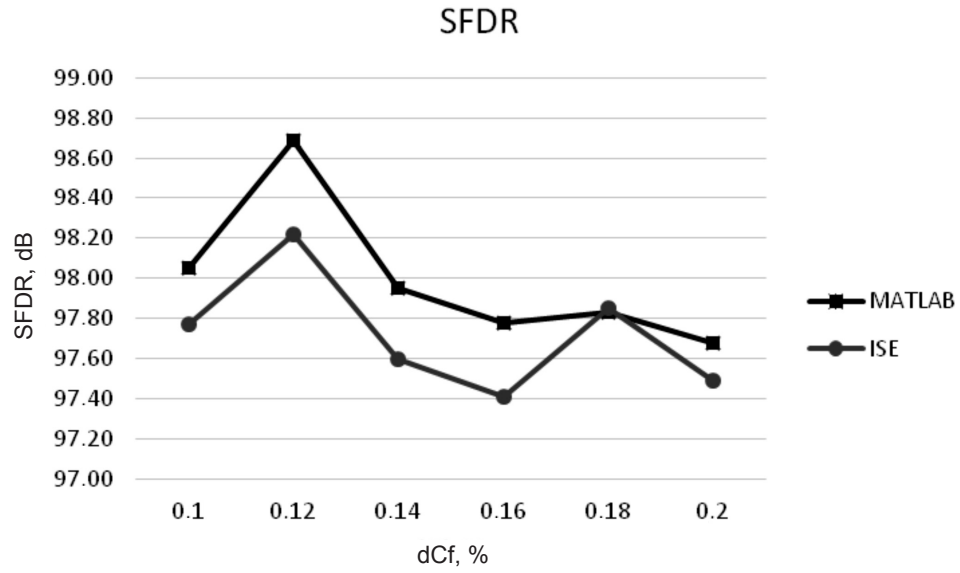

Fig. 6. SFDR after corrections in MATLAB and FPGA

The obtained results are compared with the results obtained from the LUT-based correction in MATLAB. Fig. 5 shows the values of SNDR and Fig. 6 shows the values of SFDR.

The spectra of the signal with capacitor mismatch after corrections in MATLAB and FPGA are shown in Fig. 7.

It can be seen that they are similar, which leads to the conclusion that LUT-based correction done inside the FPGA using MATLAB gives the result similar to the one obtained by MATLAB correction directly. If we consider the values, as an example let us take the capacitor mismatch of 0.14 % for DC gain of 54 dB. SNDR after MATLAB correction is 76.36 dB, after FPGA correction 76.06 dB. SFDR after MATLAB correction is 97.95 dB, after FPGA correction 97.60 dB. Therefore, it is proven that the LUT-based calibration and correction can be implemented

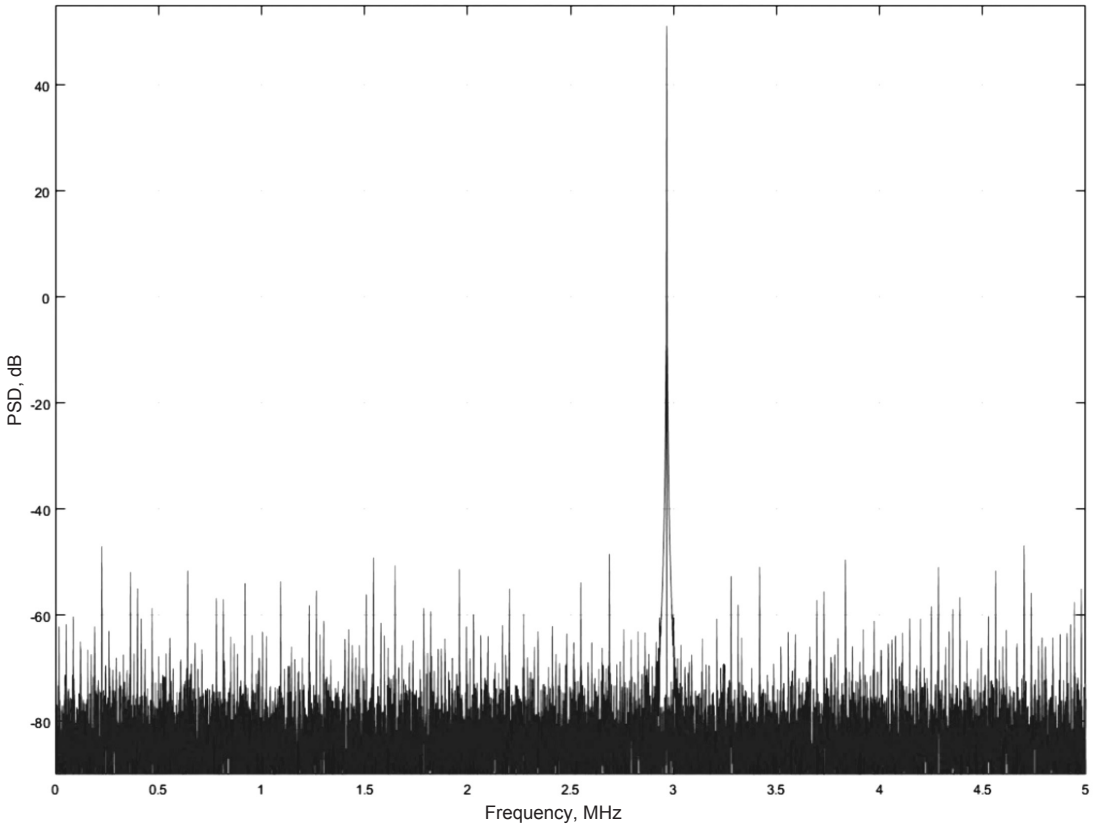

Fig. 7. Spectra after correction in MATLAB and FPGA (dC_f = 0.14 %)

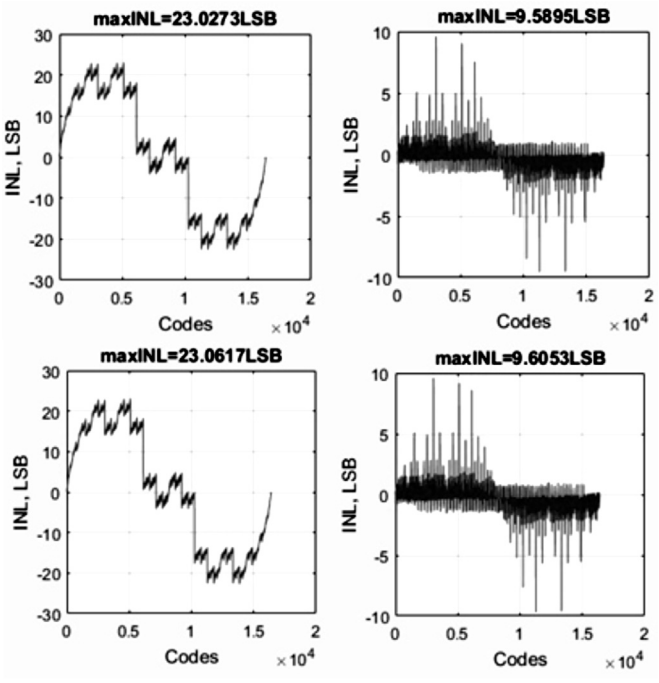

Fig. 8. INL before and after correction
in MATLAB (up) and FPGA (down), 54 dB, 0.1 %

inside the FPGA with the same efficiency as in MATLAB.

The values of INL are obtained before and after correction inside the FPGA. The values were measured for 54 dB of DC gain and 0, 0.1 and 0.2 % of capacitor mismatch. In Fig. 8 the INL characteristic before and after correction using MATLAB (up) and FPGA (down) is represented.

There is a clear improvement of INL characteristic after LUT-based corrections, performed in both MATLAB and FPGA. INL values are around 2.5 times lower than before LUT-based correction.

Conclusions

In this study, it is shown that the nonlinearity of the ADC characteristics can be removed by LUT-based calibration and correction technique. It is also shown that SNDR, SFDR and INL depend on the changes of the DC gain, as well as on the changes of the MDAC capacitors, i. e., capacitor mismatch inside the stage. Not only the simulations have been performed in this study, but the experiment as well, and the results obtained in the experiment are in good agreement with the results from simulation.

Using LUT-based calibration and correction inside the FPGA, the best results obtained in this study are the improvement of SNDR from 57.44 dB before correction to 76.98 dB after correction. For SFDR the biggest improvement obtained was from 58.12 dB to 98.22 dB. Therefore, with the LUT-based technique, SNDR can be improved for 20 dB and SFDR for 40 dB. After LUT-based correction INL is lower for around 2.5 times than before correction. Comparing the results obtained in this work with the results from the known techniques, it can be noticed that the LUT-based technique using FPGA can guarantee a similar level of improvement in SFDR, SNDR and INL, or even better.

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СВЕДЕНИЯ ОБ АВТОРАХ / THE AUTHORS

KRNETA Maja
КРНЕТА Мая
E-mail: mm.krneta@gmail.com

PIATAK Ivan M.
ПЯТАК Иван Михайлович
E-mail: i.m.piatak@gmail.com