

Research article

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DESIGN AND CONTROL OF A FAST CHARGING MODULE BASED ON THE USB-PD PROTOCOL

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Abstract. The main purpose of this article is to develop and design a USB_PD fast charging circuit based on the Type_C interface, to increase the battery life of electronic devices, provide an optimal power mode (minimum interface supply voltage of 5V while increasing the charging current). In this article, LDOs (Low Voltage Linear Regulator) are selected to implement an FPGA buck power supply, which is a fixed output regulator that provides low voltage output with current limiting, thermal shutdown, and battery reversal protection. To achieve this goal, the problems of high power consumption and low battery life caused by the rapid development of mobile devices such as mobile phones are analyzed, and it is indicated that the most effective solution at present is to increase the charging efficiency. The article briefly talks about the current state of fast charging research. The general structure of the USB PD fast charging protocol, the structure and functions of each part are analyzed. The physical layer simulation of the USB PD controller is completed using Verilog HDL, the function and implementation principle of each module is detailed, and the VCS is used for simulation to ensure that the design function is correct. The above-described board-level design is tested based on a programmable logic integrated circuit, and a logic analyzer and a protocol analyzer are used on the test results to achieve the expected design goals.

Keywords: fast charging module, USB-PD protocol, interface, Type_C, power transmission protocol

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ПРОЕКТИРОВАНИЕ И УПРАВЛЕНИЕ МОДУЛЕМ БЫСТРОЙ ЗАРЯДКИ НА ОСНОВЕ ПРОТОКОЛА USB-PD

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Аннотация. Основная цель в данной статье заключается в разработке и проектировании схемы быстрой зарядки USB_PD на основе интерфейса Type_C, для увеличения времени автономной работы электронных устройств, обеспечение оптимального режима питания (минимальном напряжении питания интерфейса 5 В при увеличении зарядного тока). В данной статье выбраны LDO (Low Voltage Linear Regulator) для реализации понижающего источника питания FPGA, который представляет собой стабилизатор с фиксированным выходом, который обеспечивает низкое напряжение, на выходе с ограничением по току, отключением при перегреве и защитой от переплюсовки батареи. Для реализации поставленной цели проанализированы проблемы высокого энергопотребления и низкого времени автономной работы, вызванные быстрым развитием мобильных устройств, таких как мобильные телефоны, и указано, что наиболее эффективным решением в настоящее время является повышение эффективности зарядки. В статье кратко рассказывается о текущем состоянии исследований быстрой зарядки. Проанализирована общая структура протокола быстрой зарядки USB PD, структура и функции каждой части. Моделирование физического уровня USB-контроллера PD завершено с использованием Verilog HDL, функция и принцип реализации каждого модуля подробно представлены, а VCS используется для моделирования, чтобы гарантировать правильность проектной функции. Выполняется проверка вышеописанной конструкции на уровне платы на основе программируемой логической интегральной схемы, а также используются логический анализатор и анализатор протоколов для анализа результатов проверки для достижения ожидаемых целей проектирования.

Ключевые слова: модуль быстрой зарядки, протокола USB-PD, интерфейс, Type_C, протокол передачи энергии

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Introduction

With the continuous digitization, the needs of applications in the field of data interaction and power transmission have further expanded. Whether it is stationary devices such as desktop computers, TVs, workstations, or portable devices such as mobile phones and tablet computers, the USB interface is undoubtedly the most direct link between data transmission and electricity [1–3]. Modern equipment not only imposes explicit requirements for increasing the data transfer rate, but also puts forward additional requirements for the throughput of the USB interface [4–6]. The ability to transfer 100W of power has become the goal that the USB 3.1 interface specification hopes to achieve, and only USB TYPE-C interface can support the transfer of this power. This requirement cannot be met according to the traditional USB

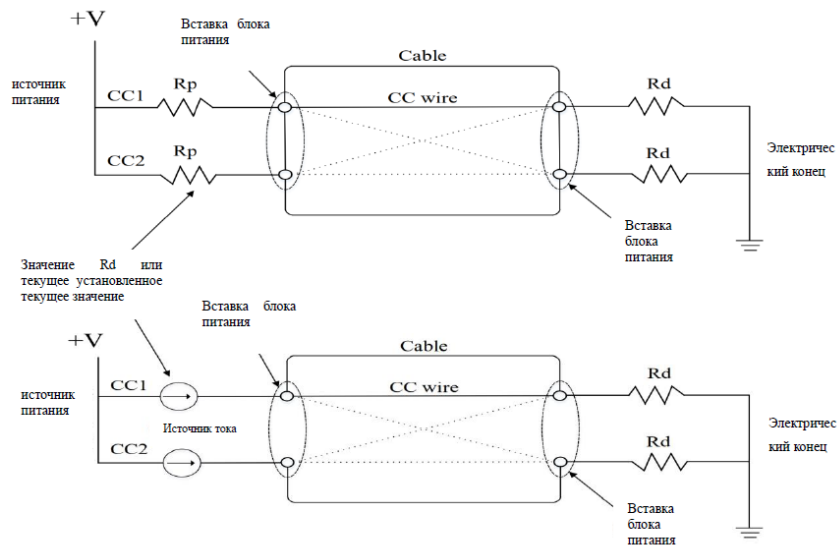


Fig. 1. Schematic diagram of intrusion detection

3.0 interface protocol specifications and below, and it is necessary to promote and apply the USB 3.1 protocol specification, which can support high power and high-speed data transmission [7–8].

With the popularization of smart devices, the performance of smartphones has become higher and higher, with more and more functions, and the hardware has improved greatly. At present, lithium batteries are mainly used in power supplies for portable electronic devices. The problem of poor device endurance is usually solved by increasing the capacity of lithium batteries. However, this method increases the weight of the device. Before lithium battery technology makes a major breakthrough, increasing its charging speed is another way to solve this problem. The fast-charging protocol is based on a certain battery capacity, reduces the charging time by increasing the charging power, and the way to increase the charging power is to start from the charging voltage and charging current. Usually there are three ways: increase the charging current while the charging voltage is unchanged, and the charging current is unchanged. At the same time, the charging voltage increases, and the charging voltage and current increase simultaneously [9–11].

Research status and development trends

The USB interface (Fig. 1) is divided into USB Type A, USB Type B, USB Type C, Mini USB, and Micro USB interfaces. The Type-C interface provides a smaller, thinner, and more durable interface instead of the traditional physical interface. Several significant advantages of the Type-C interface: The thickness of the Type-C interface is only 2.4mm, which can be used in ultra-high. In some thin devices, the Type-C interface is symmetrical, supporting the positive and negative insertion of the plug, at the same time, it also supports the positive and negative insertion of the cable direction [12–14].

The USB_PD protocol can provide a maximum power of 20V/5A for charging. Traditional USB Type_A and USB Type B interfaces cannot transmit such high power. USB_IF organization formulated USB Type_C. The interface specification stipulates that a standard data line equipped with Type_C interface can transmit a maximum current of 5A, in order to cooperate with the USB_PD fast charging protocol to achieve maximum power transfer; USB Type_C The interface is compatible with the functions of the previous generation interface, and its transfer rate can also reach 40Gbps. And there is a very convenient advantage that there is no need to distinguish the direction of the interface [15–17]. Now there are more and other devices equipped with USB Type_C interface, and interface unification is a trend, because the 100W USB_PD fast charging protocol transmission power can match the charging power of most

electronic products. Requirements and characteristics do not need to distinguish between the direction of the interface, widely used in consumer electronics such as smart phones and thin and light laptops, and will be popularized in more portable electronic devices. In the future, USB PD may use the same charger and charging cable when charging different devices, which is useful to reduce resource wastage caused by different devices having to be equipped with different chargers [18–20].

Development of the USB_PD protocol based on the Type_C interface

When the charger is charging the electric appliance, only after the charger and the electric appliance are connected stably, safe and fast charging can be done, so the insertion detection work should be the first step. As mentioned above, setting up the power supply in this design is done by connecting the CC line between the two devices. Initially, the USB Type-C VBUS interface has no power, and the system needs to connect a cable between the two devices. The role of the device is determined at connection time. A device whose CC line on a socket is pulled high is defined as a power supply terminal, and a device that goes low is defined as a power terminal.

Figure 1 shows a method for determining the role of power supply and demand, cable orientation, and current supply capability. Source terminals CC1 and CC2 are driven high through resistor R_p , and detected CC1 or CC2 is always high when nothing is connected. After connecting the power terminal, the voltage of CC1 or CC2 is reduced by the resistor R_d . Since there is only one CC wire in the cable, the source can tell which CC is low. The voltage CC1 or CC2 of the consumer is also determined. Once the CC line is detected to be high voltage, its voltage level will allow the consumer to know the current capacity of the power supply. The pull-up resistor R_p in the circuit can also be replaced by a current source that is easily implemented in an integrated circuit and can be immune to $V+$ supply voltage error.

It can be seen from the principles above that the CC line at the source end will cause voltage variations before and after switching on. In this design, two op-amp comparators op1 and op2 are used to compare the voltage changes before and after CC1 and CC2, respectively, and then according to the output signals op1out and op2out of the two op-amps, it is determined whether CC1 and CC2 are inserted [21–23].

Simulation based on programmable logic integrated circuits (FPGA)

Test plan

To make sure that the USB PD controller can work properly, you need to check the design goals with the following aspects in mind. Check if the discovery plug-in works normally and can start communicating with the PD normally after detecting the connection of the device. Whether the hardware circuit performs data processing in transmitted data packets as intended. Whether the source side and the receiver side can normally send and receive data, can they correctly analyze the received data and give appropriate feedback. The test setup in this article is to use the Alter Cyclon IV EP4CE6E22CN Development Board and the USB PD Protocol Tester (POWER-Z) as the test platform. The emulator simulates a charging terminal, and the USB PD protocol tester simulates a power consumption terminal (set to monitor mode). After the system is powered on, when the emulator detects that a device is inserted, it starts sending its own capability power supply to the tester. To facilitate observation, a logic analyzer is used to capture the waveform on the CC line, a PD protocol analyzer is used to analyze the waveform, and an oscilloscope is used to observe the voltage on the CC line during the power matching process [24–26].

If, after the test, the source terminal and the sink terminal exchange information, it means that the function of the input detection module is correct and communication with the PD starts normally. Then, by analyzing the waveform captured by the logic analyzer, when the 4b5b encoding, BMC encoding, and crc32 calculation of the transmitted data are fully realized, it indicates that the hardware circuit is working correctly. Compare the communication results output by the protocol analyzer with the overall power matching process specified in the protocol. If they match, it means that the PD communication can complete the negotiation as expected. Finally, observe the voltage on the CC line through the oscilloscope. When the voltage is 1V, indicates that the operating voltage of the CC line is normal.

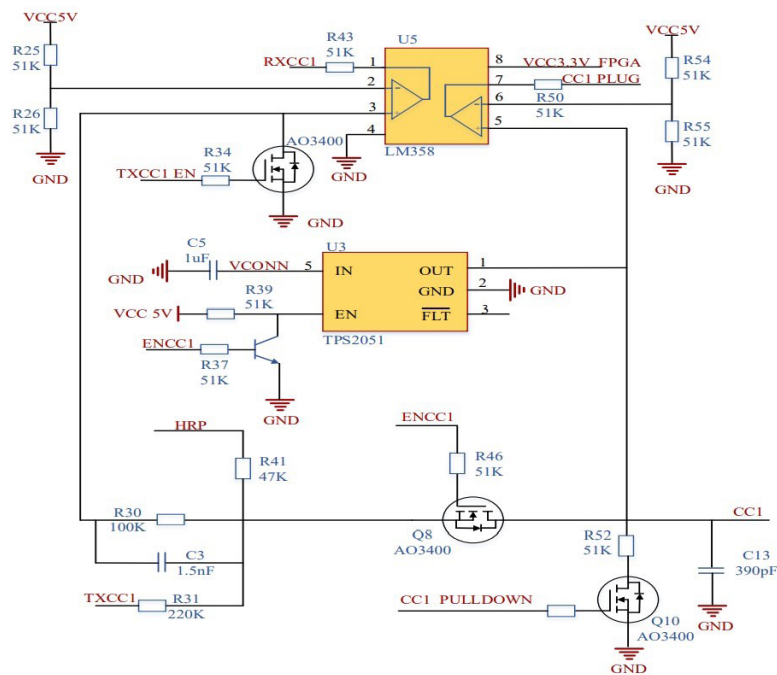


Fig. 2. CC1 Insert Detection Circuit

Construction of the test platform

The IC model chosen in this article, Alter Cyclon IV EP4CE6E22C8N, has the following features: low-cost, low-power FPGA architecture with 22320 logical cells, up to 6.3 MB of internal memory, with 80 configurable I/Os, has 4 PLLs. In this design, a stable power supply to the FPGA is achieved by choosing a model with a fixed output voltage of 3.3V [27–29].

Figure 2 shows the cable entry detection circuit in CC1. When the cable does not enter or exit, the voltage of CC1 is always at a high level. When the end of the power supply is connected, the voltage of CC1 will be pulled down, as shown in figure CC1 PULLDOWN. According to the above principle, it is only necessary to detect the voltage drop across CC1 to conclude that the cable is inserted and CC1 is valid.

The LM358 shown in the figure is a dual op-amp. Inside are two independent high-gain operational amplifiers with internal frequency compensation. [30–32]. It can effectively meet two different requirements of single power supply and dual power supply. When operating with this function, the power supply current is not affected by other factors. Voltage change detection on CC1 can be realized with LM358. When it is determined that the CC1 cable is inserted, the controller starts sending data packets to the consumer via CC1 to communicate with the PD. CC2 has the same insertion detection scheme as CC1 [33–35].

In this model, we use quartus II to write the RTL code to the FPGA. Fig. 3 shows that the RTL code was written successfully. Use the keil software to program the C code into a hex file and write it to the emulator to get an FPGA emulator that meets the test requirements, and connect the emulator to the USB PD protocol tester, logic analyzer and other equipment. construction of a verification platform. As shown in Fig. 4.

Simulation results

Using a PD protocol analyzer, the waveform represented by the logic analyzer can be analyzed fully automatically. Fig. 5 shows the entire power negotiation process resulting from the analysis of the PD protocol analyzer. After the Source is connected to the Sink, power matching occurs first via

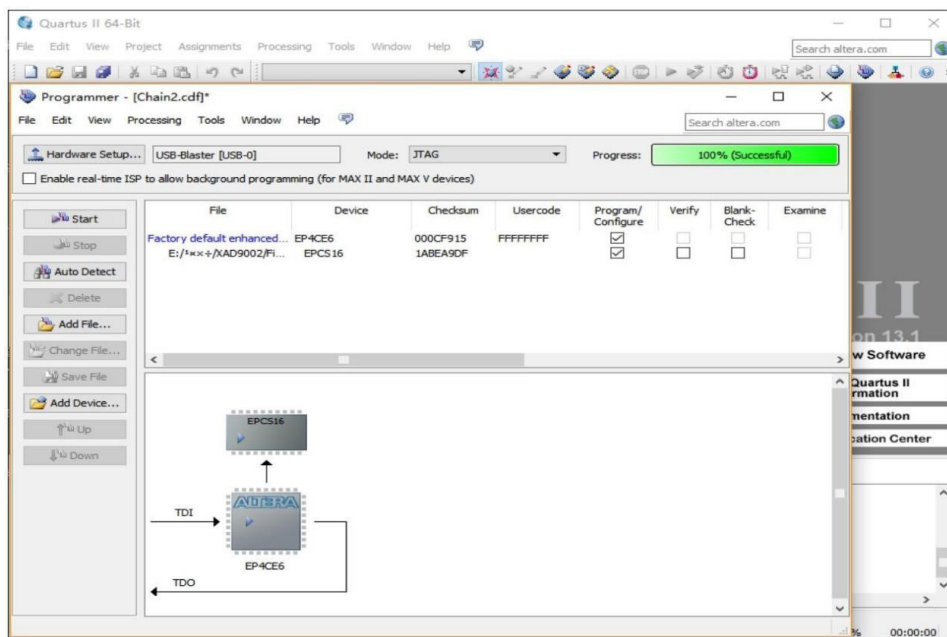


Fig. 3. Programming procedure for quartus II

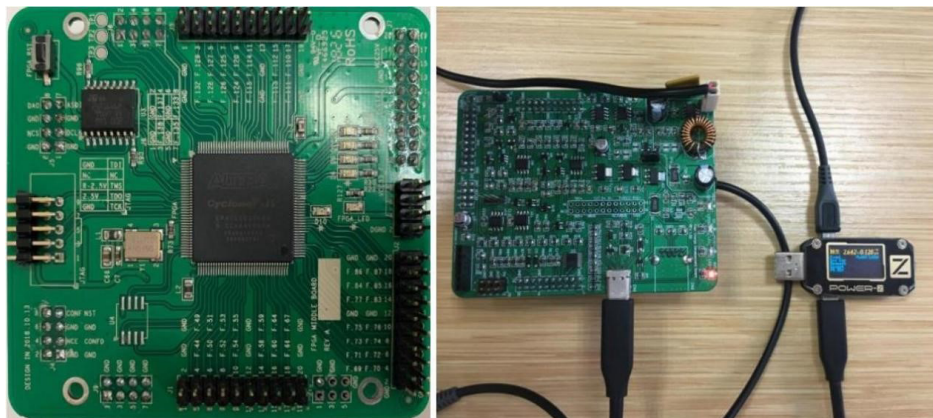


Fig. 4. FPGA Verification Platform

the CC line. Sou sends Source Cap data packets to Sink five times in a row. This data packet contains five power supply parameter specifications, namely: 5V/3.03A, 9V/2.39A, 12V/2.31A, 15V/1.91A, 20V/1.83A. After successfully receiving the Source limitation, the SINK side first returns GoodCRC data, and then parse the Source constraint and send the Request 5V/3.03A packet to the Source side, and then complete the whole process according to the communication steps of PD power negotiation. According to the above results, the PD controller can realize the expected power supply through power matching.

A fragment of the values and steps of the energy matching information is shown in Table 1.

Conclusion

The main work of this article is to simulate a charge controller that supports USB PD fast charging technology over the USB PD protocol to solve the battery life problem of electronic devices.

Table 1

Fragment of values and stages of energy matching information

Step	Source Port	Sink Port
1	The Policy Engine notifies the protocol layer to send Capabilities packets	
2	The protocol layer forwards Capability packets to the physical layer. CRCReceiverTimer start time	
3	The physical layer adds crc32 to Capabilities and sends	The physical layer receives the packet and completes the crc32 check.
4		Capabilities packets are passed from the physical layer to the protocol layer.
5		The Capability packet is passed from the physical layer to the protocol layer, which compares the ID in the received packet with the previous one and writes the new ID. The protocol layer notifies the Policy Engine that a packet has been received. The Policy Engine starts the PTransitionTimer and reduces the current. Policy Engine Starts Power Supply Transformation.
6		The protocol layer passes the GoodCRC packet to the physical layer.
7	The physical layer receives the packet and completes the crc32 check.	The physical layer adds crc32 to the GoodCRC message and
8	The physical layer passes the verified GoodCRC packet to the protocol layer, and then the protocol layer checks and updates the MessageIDCounter.	
9	The protocol layer notifies the Policy Engine Capabilities message that the message was successfully sent.	

As a result of the simulation of the operation of the PD USB controller based on a field-programmable logic integrated circuit, the optimal power mode (5V/3.03A) is realized from the 5 provided (5V/3.03A, 9V/2.39A, 12V/2.31A, 15V/1.91A, 20V/1.83A) power parameters. According to the results in the article, the PD controller can realize the expected power delivery through power matching.

REFERENCES

1. **Zhang Song, Li Yun.** FPGA Modular Design Method [J]. Journal of Electronic Measurement and Instrumentation, 28 (05) (2014) 560–565. DOI: 10.13382/j.jemi.2014.05.015
2. **Shklyarskiy Y.E., Batueva D.E.** Operation mode selection algorithm development of a wind-diesel power plant supply complex. Journal of Mining Institute, 253 (2022). DOI: 10.31897/PMI.2022.7
3. **Abramovich B.N., Bogdanov I.A.** Improving the efficiency of autonomous electrical complexes of oil and gas enterprises, Journal of Mining Institute, 249 (2021). DOI: 10.31897/PMI.2021.3.10
4. **Zhang Shiwei, Yin Shiping, He Yuntao.** FPGA control and implementation of USB2.0 interface transmission [J]. Foreign Electronic Measurement Technology, 28 (11) (2009) 74–76+80. DOI: 10.19652/j.cnki.femt.2009.11.019

5. **Li Shenghui.** Design and implementation of USB_PD protocol based on Type_C interface [D]. Xidian University, 2017.
6. **Safiullin R.N., Afanasyev A.S., Reznichenko V.V.** The Concept of Development of Monitoring Systems and Management of Intelligent Technical Complexes, *Journal of Mining Institute*, 237 (2019). DOI: 10.31897/pmi.2019.3.322
7. **Senchilo N.D., Ustinov D.A.** Method for Determining the Optimal Capacity of Energy Storage Systems with a Long-Term Forecast of Power Consumption. *Energies*, 14 (2021) DOI: 10.3390/en14217098
8. **Nurgalieva K.S., Abdullah K.A., Seyed M.A., Slavko N., John William G.G.** Application of Neural Network and Time-Domain Feature Extraction Techniques for Determining Volumetric Percentages and the Type of Two Phase Flow Regimes Independent of Scale Layer Thickness *Applied Sciences*. 12 (2022) 1–13.
9. **Ruan Yi, Song Qingliang, Wang Jia, Zhang Bingbing.** Overview and application of USB Type-C and PD technology [J]. *Integrated Circuit Applications*, 34 (04) (2017) 31–36. DOI: 10.19339/j.issn.1674-2583.2017.04.007
10. **Yu Dejun.** Research on high-power intelligent power supply technology based on USB TYPE-C protocol [D]. University of Electronic Science and Technology, 2018.
11. **Beloglazov I., Krylov K.** An Interval-Simplex Approach to Determine Technological Parameters from Experimental Data. *Mathematics*, 10 (2022). DOI: 10.3390/math101
12. **Xu Chunying, Zhao Xiaoxin, Xia Lijiao, Zhang Hongli.** Analysis of fast charging protocol and construction of test platform [J]. *Modern Telecommunications Technology*, 47 (05) (2017) 41–49.
13. **Brilliant L.S., Zavialov A.S., Danko M.U., Andronov K.A., Shpurov I.V., Bratkova V.G., Davydov A.V.** Integration of machine learning methods and geological and hydrodynamic modeling in field development design. *Neftyanoe Khozyaystvo – Oil Industry*, 3 (2022) 48–53. DOI: 10.24887/0028-2448-2022-3-48-53
14. **Wei Yongxiang, Wang Yan.** USB_PD protocol fast charging mobile power design [J]. *Journal of South China University (Natural Science Edition)*, 33 (06) (2019) 84–90. DOI: 10.19431/j.cnki.1673-0062.2019.06.015
15. **Safiullin R.N., Afanasyev A.S., Reznichenko V.V.** The Concept of Development of Monitoring Systems and Management of Intelligent Technical Complexes, *Journal of Mining Institute*, 237 (2019). DOI: 10.31897/pmi.2019.3.322
16. **Li Yong.** Emerging applications of USB PD in fast charging of mobile devices [J]. *Electronic Products World*, 25 (09) (2018) 27–30.
17. **Zhang Yi.** Research and design of fast charging controller based on USB PD protocol [D]. Xidian University, 2019. DOI: 10.27389/d.cnki.gxadu.2019.002455
18. **Brigadnov I., Lutonin A., Bogdanova K.** Error State Extended Kalman Filter Localization for Underground Mining Environments. *Symmetry*, 15 (2023). DOI: 10.3390/sym15020344
19. **Fang Kanfei.** Design and verification of fast charging control system based on USB PD protocol [D]. Anhui University, 2020. DOI: 10.26917/d.cnki.ganhu.2020.000621
20. **Sychev Y.A., Zimin R.Y.** Improving the quality of electricity in the power supply systems of the mineral resource complex with hybrid filter-compensating devices. *Journal of Mining Institute*, 247 (2021). DOI: 10.31897/PMI.2021.1.14
21. **Liu Zhongkun, Li Yeli, Lu Likun.** Design and Implementation of 4B/5B Coding Based on Oversampling CDR [J]. *Computer Applications and Software*, 32(10) (2015) 227–230.
22. **Shklyarskiy Y.E., Batueva D.E.** Operation mode selection algorithm development of a wind-diesel power plant supply complex. *Journal of Mining Institute*, 253 (2022). DOI: 10.31897/PMI.2022.7
23. **Fang Kanfei, Lin Zhiting, Zhao Jianzhong, Li Zhi, Bi Liqiang.** Design of new BMC decoding circuit for USB PD3.0 protocol [J]. *Computer Engineering and Applications*, 57 (01) (2021) 77–83.
24. **Guo Xiugen.** Talking about the evolution and future development trend of mobile phone chargers [J]. *Electronics World*, 19 (2018) 110–113. DOI: 10.19353/j.cnki.dzsj.2018.19.063
25. **Sultanbekov R.R., Beloglazov I.I., Islamov S.R., Ong M.C.** Exploring of the Incompatibility of Marine Residual Fuel: A Case Study Using Machine Learning Methods, *Energies*, 14 (8422) (2021) 1–16.

26. **Niu Yumeng, Jiao Jiye, Li Chen.** Design and implementation of FPGA-based USB PD controller [J]. Computer and Digital Engineering, 48 (05) (2020) 1238–1242.
27. **Zhang Wanrong, Wang Feihu.** Design and verification of new PD protocol chip BMC decoding circuit [J]. Electronic Technology Application, 47 (11) (2021) 29–32+38. DOI: 10.16157/j.issn.0258-7998.211493
28. **Abramovich B.N., Bogdanov I.A.** Improving the efficiency of autonomous electrical complexes of oil and gas enterprises, Journal of Mining Institute, 249 (2021). DOI: 10.31897/PMI.2021.3.10
29. **Zhu Chaocheng.** USB_PD protocol physical layer design based on TYPE_C [D]. Southeast University, 2021. DOI: 10.27014/d.cnki.gdnau.2021.003221
30. **Xue Shaojun, Wu Songlin.** PLC-based design of lifting and traversing three-dimensional garage, Electronic Production. Ser.1, 6 (2016) 13–14.
31. **Gao Jing.** Research on the hardware design of PLC-based electrical control system for threedimensional garage, Invention and Innovation (Vocational Education). 2 (2020) 146–147.
32. **Yang Shao Yang.** Application of PLC in electrical automation control, Science and technology innovation. Ser. 2, 1 (2021) 175–176.
33. **Wang Huayi.** Design of intelligent control system for three-dimensional parking garage, North China University of Technology, 8 (2019) 15.
34. **Wang Xiaonong.** Research on optimization of three-stage parking space allocation strategy for planar mobile stereo garage, Lanzhou Jiaotong University, 5 (2019) 98–100.
35. **Wu P., Pan X.L., Xu G.Y.** Research on the testing technology of relay control circuits based on digital circuit model, Ship Electric Technology. Ser.30, 4 (2010) 20–23+33.

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