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FEEDBACK ULTRA-WIDEBAND AMPLIFIER WITH UNBALANCED INPUT AND BALANCED OUTPUT

A new type of UWB LNA presents. The amplifier has got a novel feedback topology and load circuit that allows the designer to obtain a high voltage gain and matching in the wide frequency range from 3.1 GHz to 10.6 GHz without cascading, current reuse technique and an additional matching circuit. The key point of the amplifier is the source degeneration with resistive shunt series feedback and the load circuit based on the combined parallel-series resonance circuit. The voltage gain of the amplifier is 9.7 dB, matching is better than −10 dB, the noise figure lies between 5.4 and 7 dB in the whole frequency range.

CMOS; LNA; ACTIVE BALUN; UWB.

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УСИЛИТЕЛЬ С ОБРАТНОЙ СВЯЗЬЮ, НЕБАЛАНСНЫМ ВХОДОМ И БАЛАНСНЫМ ВЫХОДОМ

Представлен новый тип сверхширокополосного усилителя. Усилитель построен на основе новой топологии обратной связи и цепи нагрузки, что позволяет увеличить коэффициент усиления по напряжению и полосу согласования в широком диапазоне частот от 3,1 до 10,6 ГГц без каскадирования, техники повторного использования тока *current reuse* и без дополнительных согласующих цепей. Ключевым схемотехническим решением, использованным при построении усилителя, является одновременное введение двойной отрицательной обратной связи: индуктивной последовательной по току и резистивной параллельной по напряжению, и цепи нагрузки на основе параллельного и последовательного резонансного контура. Коэффициент усиления по напряжению усилителя 9,7 дБ, согласование лучше чем −10 дБ, коэффициент шума находится между 5,4 и 7 дБ во всем диапазоне частот.

МАЛОШУМЯЩИЙ УСИЛИТЕЛЬ; СВЕРХШИРОКОПОЛОСНАЯ РАДИОСВЯЗЬ.

Ultra-wideband (UWB) is a wireless transmission scheme that occupies bandwidth more than 500 MHz. The use of such bandwidth provides the possibility to reach high data rates for short ranges with less power consumption in comparison with conventional narrowband systems. The UWB signal can occupy bandwidth of 3.1−10.6 GHz. One of the fascinating technologies for implementation of the UWB transceiver is CMOS technology [1]. It provides a way to place RF, base-band and digital parts of the receiver on the same chip. The use of system-on-a-chip (SOC) conception allows the designer to reduce the price of the device. The UWB transceiver is formed as a combination of receiver and transmitter parts [2]. Low noise amplifier is one of the most important blocks of the receiver part as it determines the noise figure and the matching of the receiver to an antenna. The design of the LNA is a difficult task because it should strike a compromise between different characteristics of the amplifier such as power consumption, input matching, gain, noise figure, linearity and stability.

The paper describes a new approach to design the broadband low noise amplifier. This approach makes it possible to design the amplifier without techniques such as cascading

and current reuse. The idea of the approach is based on matching of the common source amplifier to source degeneration and resistive shunt series feedback. The broadening of the gain bandwidth with load circuit involves using of a parallel resonance circuit with an additional series resonance circuit. Basic amplifier topologies are presented in the second section. Different feedback topologies, matching techniques and loads are also briefly described in this section. The third section describes a novel broadband inductively degenerated common-source amplifier with shunt-series feedback and two resonance load architecture. The results of simulation are presented in the third section. The paper ends with the conclusion and the discussion of the results.

Wideband Amplifier Architecture

The amplifier should provide impedance matching of the signal source R_s (usually equal to 50 Ohm) to the combination of high-voltage gain A_V. As the CMOS amplifier is usually used in direct conversion or low IF receivers, the output of the amplifier is connected with the next receiver stage (e. g. mixer) that has high-resistance input impedance. So the CMOS amplifiers dispense with the output matching. The matching problem can be solved using different feedback and/or matching circuits. To realize a high-voltage gain the design of the appropriate load circuit is used. The circuit allows reaching high-voltage gain without additional power consumption due to effective conversion of the output current to the output voltage. The cascading leads to high power consumption [3]. The power consumption can be minimized by a current reuse technique [4]. Thus, the cascading and current reuse methods are techniques which can improve the performance of the amplifier. The amplifier presented in this work can be considered as a basic block of any LNAs. It means that the cascading and current reuse methods can be applied to this circuit as well. This is the reason why the methods will not be especially discussed. The UWB LNA can be built using common-gate or common-source circuits which are shown in Fig. 1.

The noise factor of common-gate amplifiers depends on matching conditions and has the theoretical value of 2.2 dB. In practice the minimum noise figure of this LNA type is about 3.3–4.4 dB [3, 5, 6]. Some serious disadvantage of the common-gate LNA is its relatively low transconductance that can't provide the low noise figure and high gain in a whole frequency band. So this type of the amplifier is usually used when the bandwidth does not exceed 2 GHz [5] or as the first stage of multi cascade

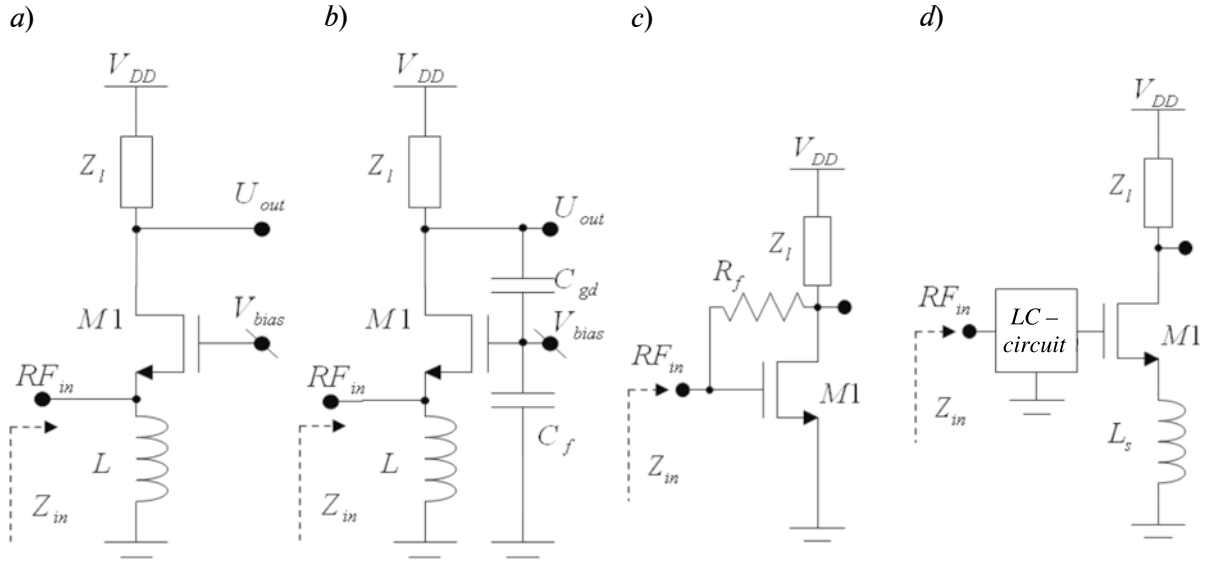

Fig. 1. The UWB LNA topologies:
a – the common-gate amplifier without feedback; *b* – the common-gate amplifier with voltage-voltage feedback; *c* – the common-source amplifier with shunt-series feedback; *d* – the common-source inductively degenerated amplifier

amplifiers where the next stages enhance the amplification bandwidth [3, 6].

The additional feedback can be used in common-gate amplifiers to dispose the dependence between the noise factor and match conditions. The common-gate amplifier can provide the real impedance equal to 50 Ohm with the higher value of transconductance by means of the voltage-voltage feedback using capacitive divider (Fig. 1 *b*) [7]. The capacitance divider is formed by capacitor parasitic gate-drain capacitance C_{gd} of the transistor $M1$ and the feedback capacitance C_f. But the frequency range of this circuit does not cover all frequency range since the voltage-voltage feedback is frequency dependent that leads to decrease of the real part of the input impedance with frequency. Another drawback of the circuit is attenuation of the input signal due to the capacitive divider formed by the gate-source parasitic capacitance of the transistor $M1$ and capacitance C_f. Thus the common-gate amplifier with capacitance feedback covers the frequency range only from 3 to 8 GHz.

Common-source stages can be used in LNAs with the so-called noise cancellation structure [8–10] or with an additional feedback circuit [11–13]. The amplifiers with noise cancellation consume much power due to the circuits consist of several stages. The noise figure is quite high due to the noise cancellation in a broad frequency range and element mismatches. The power consumption of these amplifiers is not less than 14 mW while the noise figure is not less than 4.5 dB.

Another way to reach the matching is to add shunt-series feedback (Fig. 1 *c*) using resistor R_f to common-source amplifiers [12]. But the influence of the parasitic capacitance at the output leads to increase of the real part of the input impedance $\mathrm{Re}\{Z_{in}(s)\}$ with frequency. At the same time the input capacitance leads to decrease of the value $\mathrm{Re}\{Z_{in}(s)\}$. So the frequency bandwidth of the amplifier matching is broadened with high value of transconductance despite the frequency dependence of A_V. Unfortunately the bandwidth of matching is usually limited near 5 GHz that is not enough to cover all UWB frequency range. So this type of amplifier can be used at the first stage in multi stage amplifiers due to considerable power consumption [12, 13].

The other way of achieving a broadband input matching is inductively source degenerated cascode LNA. Usually this LNA can be combined with an additional input bandpass LC-filter that neutralizes the reactive part of the input impedance across the wide frequency range [4, 14, 15] (Fig. 1 *d*). The inductively degenerated common source amplifier is obtained by adding the inductor L_s between the transistor $M1$ source and ground that forms a series resonance circuit together with parasitic gate-source capacitance C_{gs} of the transistor $M1$. This series resonance circuit also consists of resistive impedance that is equal to $g_m L_s / C_{gs}$, where g_m is transconductance of the transistor $M1$. The LC-filter at the input consists of a number of reactive elements, which can lead to larger chip area and noise figure degradation in the case of its on-chip implementation, or can lead to additional external components. Also this method suffers from the influence of parasitic capacitances and inductances due to packaging that can not be appreciated beforehand.

The input matching and the flat gain in the wide frequency band can be obtained using the so-called distributed amplifiers as well [16–18]. But it is not possible to use the distributed amplifier in a portable application due to its large power consumption (sometimes it is more than 100 mW). Also its noise figure is quite high. Sometimes it can be more than 8 dB.

Inductively Degenerated Common-Source Amplifier with Shunt-series Feedback and Two Resonance Load Circuit

Designing a low noise amplifier for UWB radio in the frequency range of 3.1–10.6 GHz based on CMOS technology needs choosing a feedback configuration of the LNA that can provide simultaneously good input matching, high gain and low noise. The proposed circuit based on the source degenerated amplifier with shunt series feedback. As it is shown in Fig. 2, the common source amplifier with shunt series feedback provides matching in a low frequency range (Fig. 2 *a*) and the source degenerated amplifier provides matching at the frequency band near the resonant frequency of the series tank by inductance L_g and gate-source

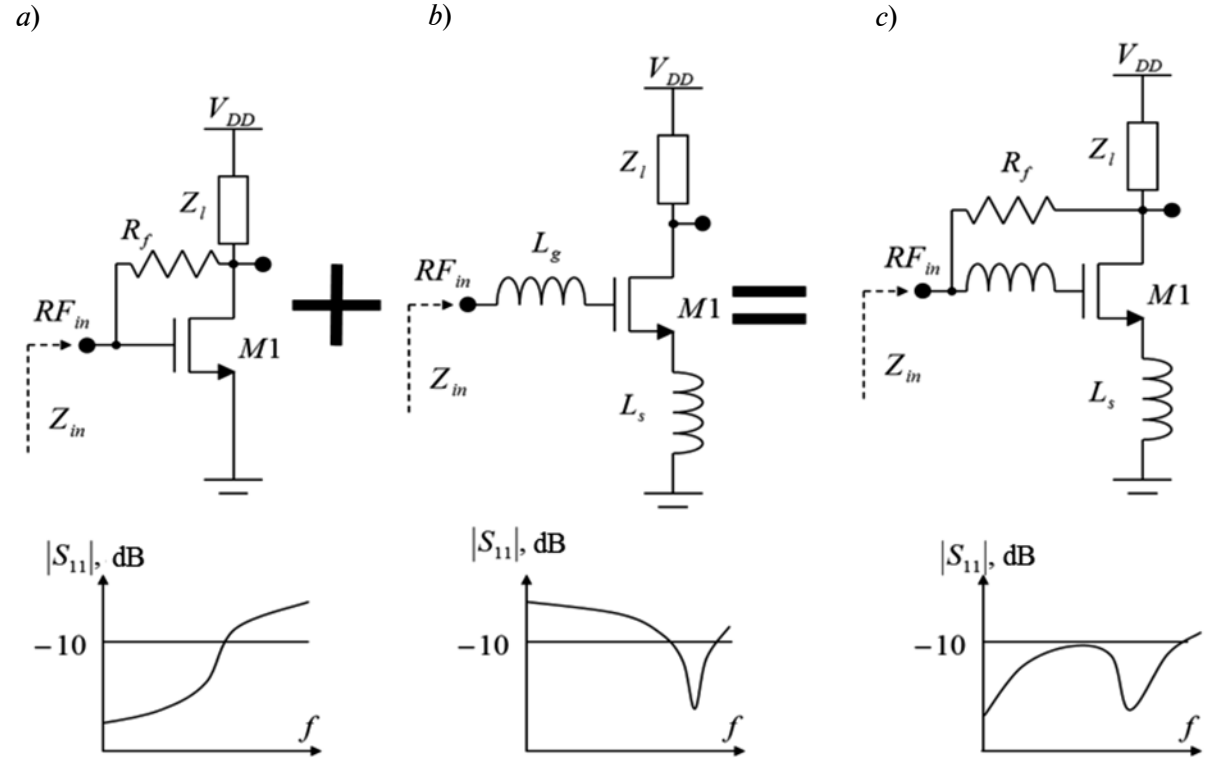

Fig. 2. The amplifier topologies and its $S11$ parameter absolute value vs. frequency: a – the common-source amplifier with shunt-series feedback; b – the common-source inductively degenerated amplifier; c – the proposed common-source amplifier with dual feedback

capacitance of transistor $M1$ (Fig. 2 b). So the combination of two types of feedback can considerably broaden the frequency band of the amplifier because the matching band broadens as well (Fig. 3 c).

So the matching task can be formulated as the following inequality using the reflection coefficient Γ with acceptable level −10 dB

$$|\Gamma| \approx |S_{11}| = \left|\frac{Z_{in}(s,\mathbf{M}) - R_s}{Z_{in}(s,\mathbf{M}) + R_s}\right| < -10\,\text{dB}, \quad (1)$$

where Z_{in} is the input impedance; R_s – source resistance; s – complex frequency; $\mathbf{M}$ is the vector of the element values.

This inequality should be fulfilled in the desired frequency range and can have a multitude of solutions. But in this case the solution that provides the maximum voltage gain, $A_{V\max}$, should be chosen. So the (1) should be solved together with the next condition:

$$A_{V\max} \approx \left|S_{21}(\mathbf{M}_{opt})\right| = \max\left|S_{21}(s,\mathbf{M})\right|, \quad (2)$$

where $\mathbf{M}_{opt}$ is the vector of element values which leads to maximum of the voltage gain. The symbolic solution of this set is not possible. Therefore the element values should be obtained using numerical optimization.

Let us consider the full circuit of the amplifier that was designed using the proposed feedback topology. The described procedure provides the possibility to obtain the parameters of the amplifier circuit shown in Fig. 3 a. The first stage of the circuit is the amplifier with a dual feedback; the second stage is an active balun with unity voltage gain. The amplifier is designed to work on the capacitance load of the next stage.

It is based on the cascode stage that consists of the transistors $M1$–$M3$. The equivalent width of transistors pair $M1$, $M2$ is two times as large as transistor $M3$ to increase transconductance of transistor pair $M1$, $M2$ and minimize the gate-source capacitance of $M3$. The source degeneration inductance is formed by a parallel connection of the planar inductor $L1$ and $L2$ to decrease the total inductance to cover large frequency band. The

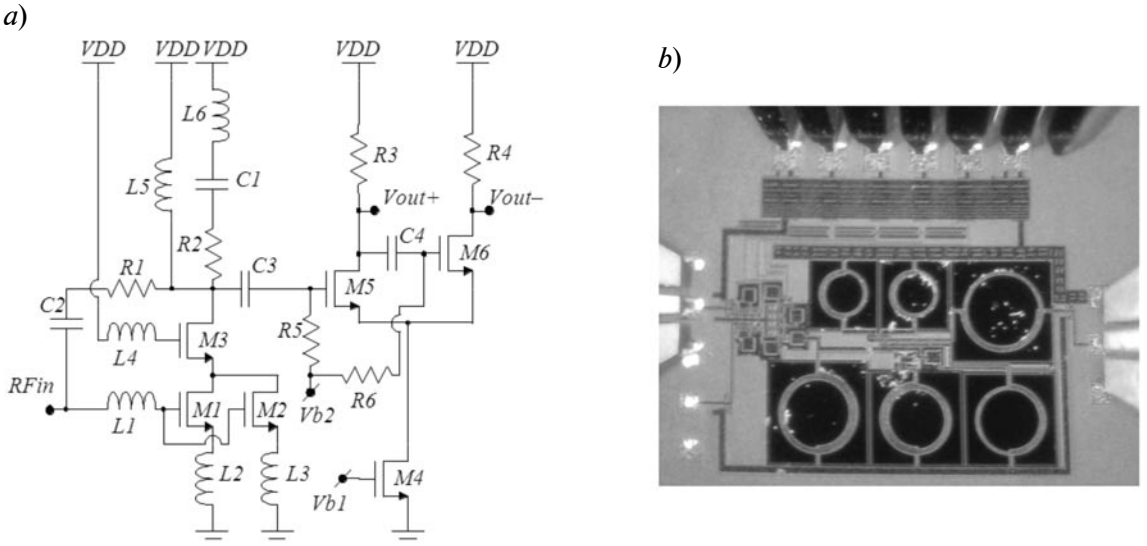

Fig. 3. The proposed feedback ultra-wideband lownoise amplifier:
a – circuit; *b* – chip photography through a microscope

planar inductor *L*1 resonates with the gate-source capacitance of transistors *M*1 and *M*2. The shunt-series resistor *R*1 provides matching in low frequency range. The planar inductor *L*4 boosts the transconductance of the transistor *M*3 in the high frequency range. The circuit load is implemented by means of elements *L*5, *L*6, *C*1, *R*2 to provide flat voltage gain in the whole frequency range. The load is based on inductor *L*5 that resonates with the parasitic capacitance *C* at the output of the first stage of the amplifier. In contrast to the different bandwidth extension techniques, for example described in [19], the inductor *L*5 with the series *RLC*-circuit constructed from elements *L*6, *C*1, *R*2 are used to increase the voltage gain in desired frequency band that is far from zero frequency. This series circuit introduces the second resonance frequency of the load impedance. In addition, *L*5 allows biasing the amplifier without loosing of voltage swing. The transistors *M*4–*M*6 and resistors *R*3–*R*4 form the active balun to convert the single ended signal to differential form. The other passive elements are used for biasing and coupling of ac and dc signals. The load is based on inductor *L*5 that resonates with the parasitic capacitance *C* at the output of the first stage of the amplifier. In contrast to the different bandwidth extension techniques, for example described in [19], the inductor *L*5 with the series *RLC*-circuit constructed from elements *L*6, *C*1, *R*2 are used to increase the voltage gain in desired frequency band that is far from zero frequency. This series circuit introduces the second resonance frequency of the load impedance.

The LNA design procedure should include the influence of the passive element parasitics, because the parasitic elements, especially inductors, cause performance degradation effects of the circuit at high frequency range. So the optimization incorporated in circuit simulation programs should be used. The parameters of optimization are the values and the geometric sizes of passive elements. The optimization task is formulated as follows:

maximization of $|S_{21}|_{\max}$ in the frequency range 3.1–10.6 GHz;

fulfillment of $|S_{11}|_{\max} < -10$ dB in the frequency range 3.1–10.6 GHz;

fulfillment of the gain flatness $|S_{21}|_{\max} - |S_{21}|_{\min} < 3$ dB in the frequency range 3.1–10.6 GHz, where the $|S_{21}|_{\max}$, $|S_{21}|_{\min}$ are the highest and lowest absolute values of S_{21} consequently, $|S_{11}|_{\max}$ is the highest absolute value of S_{11} in desired frequency range.

The amplifier elements were calculated during the optimization and simulation as equivalent subcircuits. These equivalent subcircuits describe the elements in frequency range till 20 GHz. The amplifier has got

the following simulated characteristics: the reflection coefficient is less than −10 dB in the frequency band from 3.1 to 10.6 GHz, the maximum absolute value of the voltage gain is 9.7 dB and the noise figure is ranging from 5.4 to 7.0 dB. The first stage consumes 4.2 mA from the 1.8 voltage source, the second one − 12 mA. The element parameters and characteristics were obtained by optimization and simulation using the Cadence Virtuoso custom design IC platform.

As a result all transistors $M1-M5$ were realized as a multi finger structure with an equivalent dimension of the W/L equal to 105 um/0.18 um. The inductors $L1$, $L2$, $L3$, $L4$, $L5$, $L6$ are spiral planar inductors. The inductors $L2$ and $L3$ have turn number 1.5 and the internal diameter 126 um with the inductance about 0.57 nH. The inductor $L1$ has the inductance about 1.3 nH by turn number 1.5 and internal diameter 227 um. The inductor $L5$ and $L6$ have inductances 2.9 and 2.0 nHn consequently by turn number 2.5 and internal diameter 210 um and 200 um consequently. The feedback resistor $R1$ with resistance 300 Ohm and load resistor $R2$ with resistance 200 Ohm are P+ poly resistors. The resistors $R3$ and $R4$ are 50 Ohm P+ poly resistors.

The described amplifier was implemented using UMC CMOS 180 nm as a standalone chip and its chip photography through a microscope is shown on Fig. 3 *b*. For the measurement purpose the ESD protection circuit and two buffers with the gain minus 6 dB were added on the outputs of the amplifier to drive 50 Ohm external load.

The results of the circuit simulation of the chip using the Cadence Virtuoso custom design IC platform, on-wafer measurement using network analyzer Rohde & Schwarz ZVA40, probe station Cascade Microtech EP6RF are shown in Fig. 4.

The parameter $|S11|$ is presented in Fig. 4 *a*. As we can see $|S11|$ is less then −10 dB in the frequency range 3.0−9.8 GHz that is in a good accordance with the results of simulations. Its minimum is on the frequency of 8 GHz and is equal to −25 dB. The parameter $|S21|$ (Fig. 4 *b*) defines the gain of the amplifier. Its maximum value is near 3.4 dB and lies in the frequency 3 GHz. The experimental results show that the matching bandwidth is on the frequency range of 2.4−8.4 GHz by the level −20 dB with the minimum value of $|S11|$ −30 dB

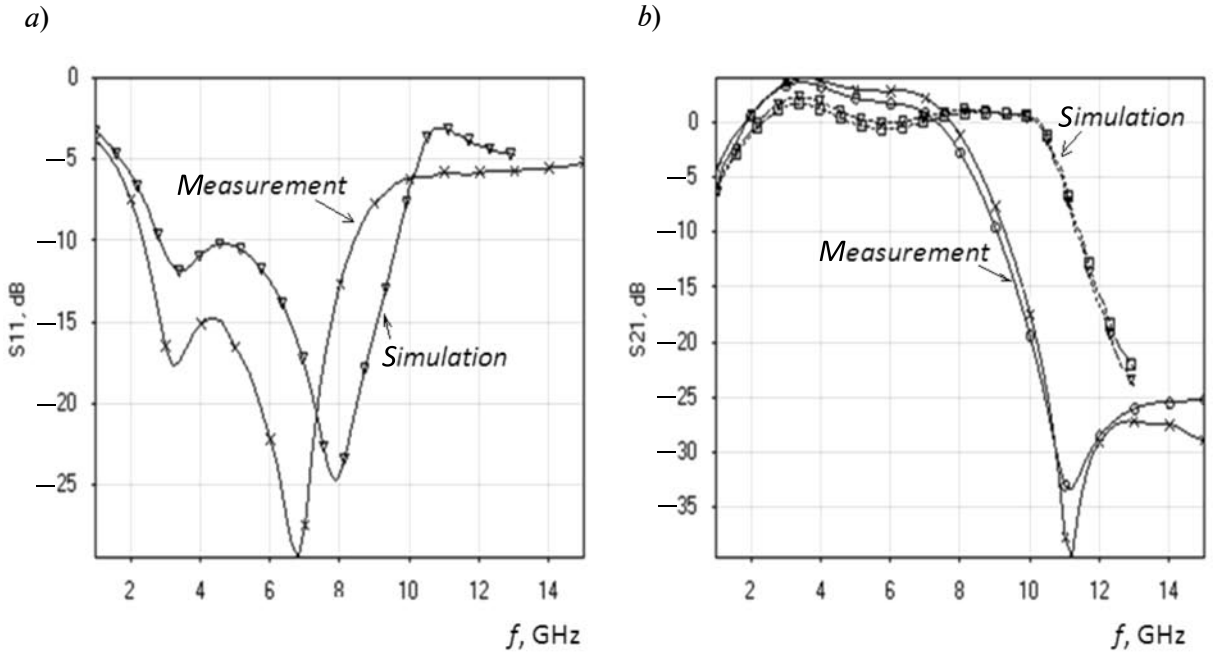

Fig. 4. The measurement and simulation results:
a − the dependence of |S11| vs. frequency; *b* − the dependence of |S21| vs. frequency on the balanced outputs

on the frequency 7.0 GHz. The experimental results show that the maximum of |*S*21| parameter is 4 dB on the frequency 3 GHz and the amplification bandwidth is 2.0–7.5 GHz.

The difference between the measurement and simulation is the result of technological parameter dispersions. Although the parameters |*S*11| and |*S*21| are close to simulations in the frequency band till 8 GHz, it confirms the efficiency of the proposed scheme. It also shows that the gain would be 6 dB higher without matching buffers how it was predicted by simulations. The |*S*11| dependence vs. frequency character with to minimum on the graph (Fig. 4 *b*) that was predicted (expected) also confirms the efficiency of the proposed feedback architecture of the amplifier. As we can see, the |*S*21| dependence vs. frequency measured on the balanced outputs of the amplifier is quite close to each other (Fig. 4 *b*). Thus the use of the active balun is an efficient solution to obtain a balanced signal that is necessary for the frequency conversion at the next stage.

In this paper we come to the conclusion that the proposed LNA differs significantly from the amplifiers published in recent years. The described method is based on the use of the shunt-series feedback to match the LNA in low frequency band and the use of the inductive degeneration to match the LNA in high frequency band. The active balun is used to convert the unbalanced signal to the balanced form. The parameters of the LNA are compared with parameters of low noise amplifiers described earlier in the literature. So the amplifier has got the following characteristics: the reflection coefficient is less than required value –10 dB in the frequency band from 3.1 to 10.6 GHz, the maximum value of the voltage gain is 9.7 dB and the noise figure is ranging from 5.4 to 7.0 dB. The first stage consumes 4.2 mA, while the second stage consumes 12 mA from the 1.8 voltage source. Thus, the results proved by the comparison of simulation and experimental results show that the simulation and measurement are quite close in frequency band till 8 GHz.

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