DOI: 10.18721/JCSTCS.13404
УДК 621.396.6

SUB-6 GHz IP BLOCKS FOR 5G TRANSCEIVERS IN 65 nm CMOS

I.A. Rumyancev

Peter the Great St. Petersburg Polytechnic University,
St. Petersburg, Russian Federation

This paper presents the development results of a vector modulator, a low-noise amplifier and a power amplifier for the 4.80–4.99 GHz. It is planned to deploy fifth-generation communication systems in this frequency band in the Russian Federation. Circuits, layouts and simulation results of the designed IP blocks are presented and compared with state-of-the-art works. All circuits are inductorless to improve bandwidth and reduce the layout area. Thus, the vector modulator area, which has the largest dimensions, is only 0.4 sq. mm. The use of a vector modulator that combines the functions of an attenuator and a phase shifter in the transceiver modules makes it possible to calibrate the amplitude-phase states to minimize the influence of the technological process parameters variation. According to the simulations results, the designed IP blocks allow implementing the transceiver for the whole sub-6 GHz band (3–5 GHz).

Keywords: vector modulator, power amplifier, low noise amplifier, CMOS, calibration, 5G.

Citation: Rumyancev I.A. SUB-6 GHz IP blocks for 5G transceivers in 65 nm CMOS. Computing, Telecommunications and Control, 2020, Vol. 13, No. 4, Pp. 44–53. DOI: 10.18721/JCSTCS.13404

IP-БЛОКИ ДЛЯ ПРИЁМОПЕРЕДАТЧИКОВ СЕТЕЙ 5G НА ОСНОВЕ 65 нм КМОП-ТЕХНОЛОГИИ

И.А. Румянцев

Санкт-Петербургский политехнический университет Петра Великого,
Санкт-Петербург, Российская Федерация

В статье представлены результаты разработки интегральных схем векторного модулятора, малошумящего усилителя и усилителя мощности для приёмопередающих модулей диапазона частот 4,80–4,99 ГГц, в котором планируется развертывание систем связи пятого поколения в Российской Федерации. Представлены принципиальные схемы, топологии и результаты моделирования IP-блоков, проведено сравнение полученных характеристик с аналогичными разработками. Разработанные интегральные схемы не содержат индуктивных элементов, что позволяет значительно расширить полосу рабочих частот и уменьшить площадь топологии. Так, площадь топологии векторного модулятора, имеющего наибольшие габариты, составляет всего 0,4 кв. мм. Использование векторного модулятора, объединяющего в себе функции аттенюатора и фазовращателя, в приёмопередающих модулях позволяет обеспечить возможность калибровки амплитудно-фазовых состояний для минимизации влияния разброса параметров технологического процесса. Согласно результатам моделирования, на основе разработанных IP-блоков можно реализовать универсальный приёмопередатчик для всего диапазона до 6 ГГц (3–5 ГГц) систем 5G.

Ключевые слова: векторный модулятор, усилитель мощности, малошумящий усилитель, КМОП-технология, калибровка, 5G.

Ссылка при цитировании: Румянцев И.А. IP-блоки для приёмопередатчиков сетей 5G на основе 65 нм КМОП-технологии // Computing, Telecommunications and Control. 2020. Vol. 13. No. 4. Pp. 44–53. DOI: 10.18721/JCSTCS.13404

Introduction

The fifth generation (5G) communication systems, in comparison with the existing ones, have significant advantages, such as lower latency, higher data rates and connection density, better energy and spectral efficiency [1]. To provide these benefits, multiple frequency bands and electrically scanned antennas are used. According to GSMA information, the frequency spectrum of 5G systems is divided into three bands [2]: sub-1 GHz (~ 600–700 MHz), sub-6 GHz (~ 3–5 GHz) and above 6 GHz (~ 24–29 GHz and higher). However, specific frequency ranges in these bands may differ from country to country. In the Russian Federation the 4.80–4.99 GHz range is allocated for the 5G in the sub-6 GHz band [3], while in most other countries the 3.4–3.8 GHz range will be used.

There are three main electronically scanned antenna architectures [4]: digital, analog and hybrid. The last two use phase shifters (PS) as a key element. A hybrid architecture that combines analog and digital parts is considered by the scientific community and commercial companies as the most promising due to the higher flexibility compared to pure analog architecture and lower power consumption compared to purely digital architecture. Among the possible ways to build hybrid electronically scanned antenna, two approaches can be distinguished:

- based on high power amplifiers with power dividers/adders and phase shifters;
- based on many transceiver modules with low and medium power amplifiers.

The first approach seems promising due to fewer power amplifiers. However, in practical implementation problems associated with high insertion losses of power splitters/combiners and GaAs or GaN phase shifters. The second approach is more complicated, but allows to process low power RF signals by silicon integrated circuits and then amplify them if necessary [5]. Silicon technology makes it possible to integrate RF circuits with mix-mode circuits, such as analog-to-digital converters [6, 7] and digital-to analog converters [8], and with digital circuits in one die. Digital circuits can also be implemented in GaAs, but with lower energy efficiency [9]. Thus, the development of silicon IP blocks for the 5G transceiver modules in the 4.80–4.99 GHz range is an urgent task, the solution of which is presented in this paper.

CMOS RF IP blocks: circuits, layouts, simulation and comparison

The designed low noise amplifier (LNA) circuit is shown in Fig. 1*a* and consists of an input amplifier based on a feedback inverter, an active balanced-to-unbalanced signal converter, and a common-source output stage. The LNA is implemented on the basis of the noise canceling technique [10] to ensure low noise figure in a wide frequency range. The dimensions of the LNA layout are 150 x 335 um (Fig. 1*b*).

The results of computer simulation after parasitic parameters extraction are shown in Fig. 1*c*. Taking into account the influence of the input bonding wire, the developed low-noise amplifier in the frequency band of 1.1–7.7 GHz provides a gain of 12.2–15.2 dB, a noise figure (NF) of 2.45–2.80 dB, an input and output return losses better than –10 dB.

In the 4.80–4.99 GHz range, the forward transmission coefficient S21 is more than 13.8 dB, the noise figure is below 2.53 dB, the input and output return losses are below –20.4 dB and –13.4 dB consequently. The power consumption of the circuit is about 14.4 mW with the input 1 dB compression point –21.4 dBm. The performance comparison of the designed low-noise amplifier with similar solutions is presented in Table 1.

The designed two-stage power amplifier circuit is shown in Fig. 2*a*. Each stage is based on a pair of *N*-transistors in a cascode connection to double the circuit supply voltage and increase the output power

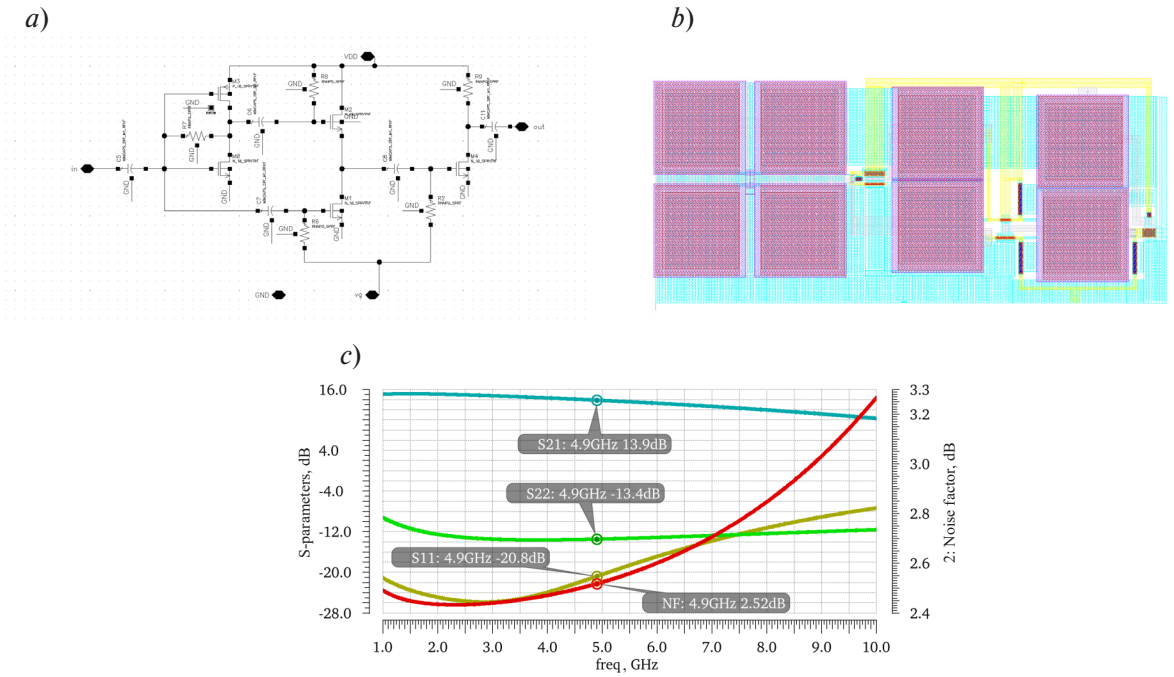

Fig. 1. Low noise amplifier schematic (*a*), layout (*b*), *S*-parameters and NF versus frequency (*c*)

Table 1

Performance Comparison of the LNAs

	[11]	[12]	[13]	[14]	[15]	[16]	This work
Technology, nm	180	130	180	350	130	180	65
Frequency, GHz	3–10	0.2–3.3	3.4–3.8	3.3–3.8	2.3–2.7	2.0–5.0	1.1–7.7
Gain, dB	11	13.8	15.3	23.1	18.7	14.9	15.2
Input CP1dB, dBm	–15	–19.6*	–13.5	–18	–17.2	–12.0	–21.4
Power consumption, mW	11.5	19.0	9.3	27.6	9.4	14.0	14.4
NF, dB	3.2	3.4	1.35	2.5	0.85	3.2	2.8
Area, sq. mm	N/A	0.15	N/A	N/A	N/A	1.35	0.05

*Estimated

level. The dimensions of the power amplifier layout are 280 x 190 μm (Fig. 2*b*). The results of computer simulation after parasitic parameters extraction are shown in Fig. 2*c* and Fig. 2*d*. Taking into account the influence of the output bonding wire, the power amplifier in the 2.0–15.9 GHz frequency range provides 24.1–24.7 dB gain with the input and output return losses better than –10 dB. In the frequency range of 4.80–4.99 GHz, the input 1 dB compression point is better than –10.0 dBm, while the output power is 13.9 dBm with 13.3% power-added efficiency (PAE). The state-of-the-art linear power amplifiers characteristics comparison is given in Table 2.

The block diagram of the developed vector modulator is shown in Fig. 3*a* and consists of an input active balun (UnBal) that converts an unbalanced signal to a balanced form, a second-order passive polyphase

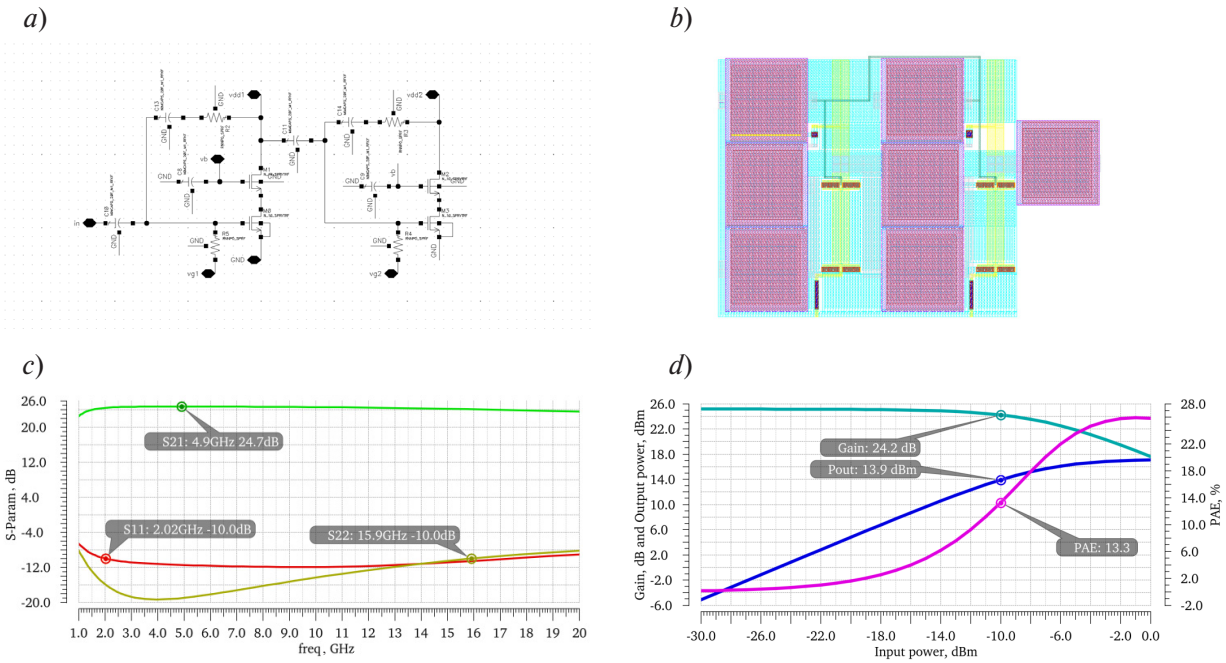

Fig. 2. Power amplifier schematic (*a*), layout (*b*), *S*-parameters versus frequency (*c*), gain, output power and PAE versus input power (*d*)

Table 2

Performance Comparison of the Power Amplifiers

	[17]	[18]	[19]	[20]	[21]	[22]	This work
Technology, nm	180	65	65	180	130	180	65
Frequency, GHz	3.1–10.6	2.5–2.6	2.4	1.8–2.6	6.0–9.0	3.0–10.6	2.0–15.9
Gain, dB	15	30	13.5	22	8	11.5	24
Output CP1dB, dBm	4.3	22*	6	21*	7	9	14
Power consumption, mW	14.4	1250	171	818	22	34	189
PAE, %	18	12.6	2.4	15.4	22.7	23.5	13.3
Area, sq. mm	0,53	2.98	1.7	1.33	0.86	0.81	0.05

*Estimated

RC filter (PPF), an adder based on Hilbert cells, an output active converter from a balanced signal to an unbalanced signal (Balun) and an output amplifier. Schematics of the listed circuits are presented in [23]. The dimensions of the vector modulator layout are 1050 x 410 μm (Fig. 3*b*).

The developed vector modulator has a maximum gain of 10.7 dB. In the frequency range of 4.80–4.99 GHz, the transmission coefficient of the circuit varies from minus 0.1 dB to plus 0.5 dB. The input 1 dB compression point is about –5 dBm while the power consumption of the circuit is less than 40 mW. The calibration procedure [24] has been performed to obtain 6 bit phase resolution and 5 bit amplitude resolution. The designed modulator controls gain from 0 dB to –8 dB with 0.5 dB steps. Simulation results of the vector modulator gain and phase versus frequency are presented in Fig. 3*c* and Fig. 3*d* respectively. The maximum amplitude and RMS phase errors calculated from the simulation

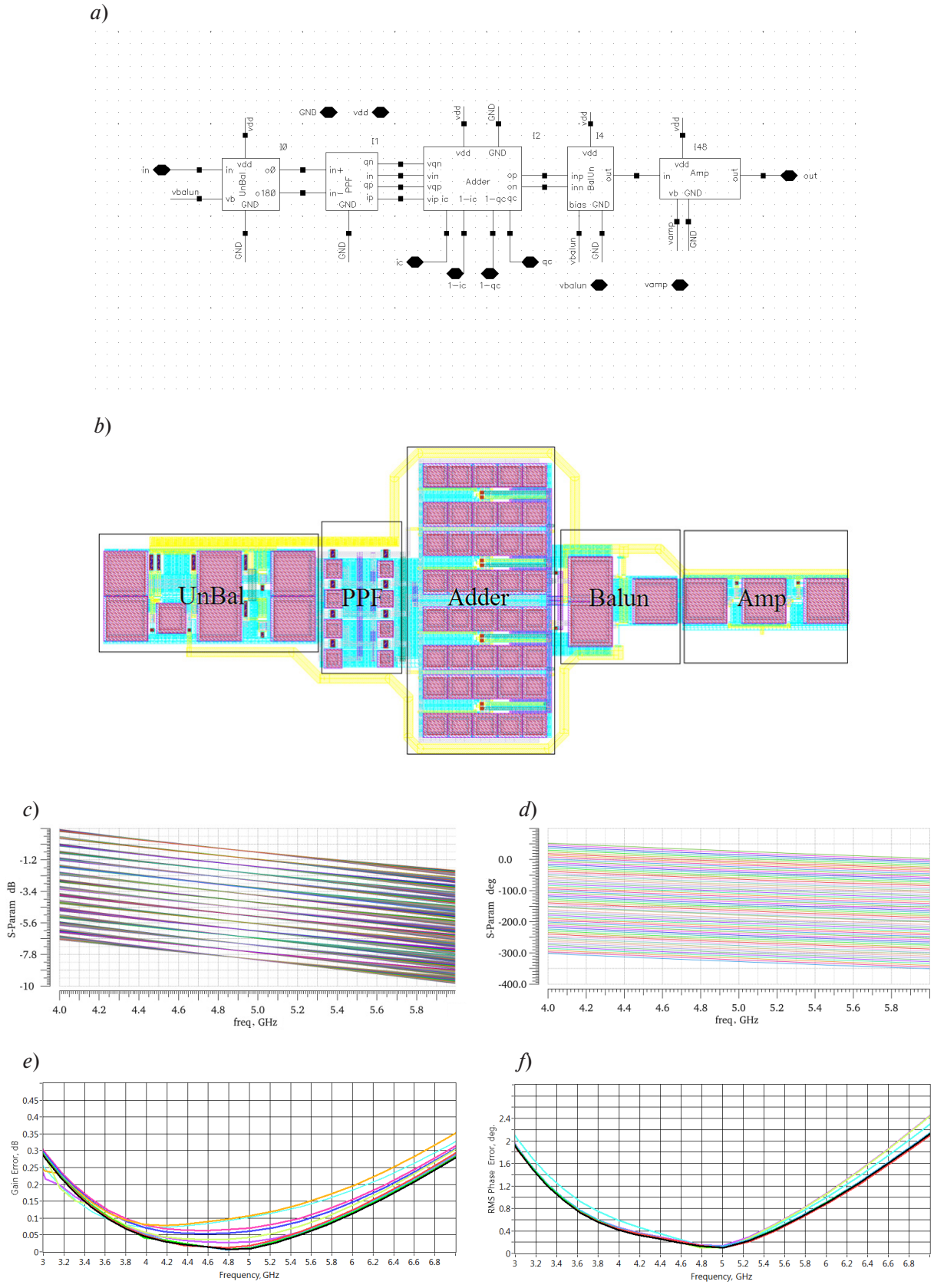

Fig. 3. Vector modulator block diagram (*a*), layout (*b*), simulated gain (*c*) and phase (*d*) versus frequency, calculated gain (*e*) and phase (*f*) errors versus frequency

Table 3

Performance Comparison of the PSs and VMs

	[25]	[26]	[27]	[28]	[29]	[30]	[31]	This work
Technology, nm	130	180	180	180	180	180	180	65
Frequency, GHz	0.5–6.0	1.0–2.1	2.3–4.8	0.8–2.7	2–3	2.2–3.2	2.8–3.2	3.2–5.0
Phase error, deg.	7.0	N/A	1.4	7.2	5.0	4.5	1.0	2.2
Gain error, dB	1.0	1.5	1.1	0.8	1.5	1.1	0.4	0.4
Gain, dB	8.0	4.8	–3.0	–17.4	0	–6	1.7	~ 0
Power consumption, mW	28	5	19	21	24	95	99	40
Input CP1dB, dBm	–22	–2	0.6	N/A	–14	4	4	–5.2
Area, sq. mm	1.3	0.3	0.9	0.9	0.4	6.0	5.3	0.4

results are presented in Fig. 3*e* and Fig. 3*f*. As can be seen from the data the designed circuit can be used in the whole sub-6 GHz band if it will be calibrated in the middle of this band. Table 3 summarizes the performance of the designed vector modulator and presents a comparison with similar solutions.

Conclusion

This paper presents a low noise amplifier, power amplifier and vector modulator for sub-6 GHz 5G systems in 65 nm CMOS technology. Due to inductorless structure, the designed blocks are broadband and occupy small silicon area (0.05–0.4 sq. mm) while providing competitive characteristics. Based on the proposed IP blocks, the universal transceiver module for sub-6 GHz 5G band (3–5 GHz) can be designed.

Acknowledgment

This work was financially supported by the Russian Science Foundation (project № 19-79-00329).

REFERENCES

1. 5G Spectrum Public Policy Position. Available: *http://www-file.huawei.com/-/media/corporate/pdf/public-policy/public_policy_position_5g_spectrum.pdf* (Accessed: 02.02.2021).

2. 5G Spectrum GSMA Public Policy Position. Available: *https://www.gsma.com/spectrum/wp-content/uploads/2020/03/5G-Spectrum-Positions.pdf* (Accessed: 02.02.2021).

3. Vydeleny polosy dlya sozdaniya pilotnykh zon setey svyazi 5G. Available: *https://digital.gov.ru/ru/events/38690/* (Accessed: 02.02.2021). (rus)

4. **Rumyancev I.A., Korotkov A.S.** Survey on beamforming techniques and integrated circuits for 5G systems. *IEEE International Conference on Electrical Engineering and Photonics (EExPolytech)*, St. Petersburg, Russia, 2019, Pp. 76–80. DOI: 10.1109/EExPolytech.2019.8906842

5. **Peterson B., Schnaufer D.** 5G fixed wireless access array and RF front-end trade-offs. *Microwave Journal*, 14 Feb. 2018, Pp. 1–9.

6. **Pilipko M.M., Manokhin M.E.** Design of a low-power 12-bit SAR ADC. *IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus)*, St. Petersburg, Russia, 2019, Pp. 129–131. DOI: 10.1109/EIConRus.2019.8657039

7. **Budanov D.O., Morozov D.V., Pilipko M.M.** An 8-bit analog-to-digital converter with a novel encoder using 90 nm CMOS. *IEEE International Conference on Electrical Engineering and Photonics (EExPolytech)*, St. Petersburg, 2018, Pp. 56–59. DOI: 10.1109/EExPolytech.2018.8564441

8. **Enuchenko M.S., Morozov D.V., Pilipko M.M.** An 8-bit parallel DAC with segmented architecture. *J. Commun. Technol. Electron.*, 2017, No. 62, Pp. 89–100. DOI: 10.1134/S1064226917010053

9. **Stesev G., Budanov D., Balashov E.** Serial-to-parallel converter using GaAs D-Mode transistors. *IEEE International Conference on Electrical Engineering and Photonics (EExPolytech)*, St. Petersburg, Russia, 2020, Pp. 67–70. DOI: 10.1109/EExPolytech50912.2020.9243862

10. **Balashov E.V., Korotkov A.S.** Radio frequency CMOS low noise amplifiers: application, circuit design, and progress trends. *Uspekhi sovremennoy radioelektroniki* [*Achievements of Modern Radioelectronics*], 2007, No. 2, Pp. 3–34. (rus)

11. **Balashov E.V., Korotkov A.S.** Ultra wideband low noise amplifier with source degeneration and shunt series feedback. *4th European Conference on Circuits and Systems for Communications*, Bucharest, Romania, 2008, Pp. 87–92. DOI: 10.1109/ECCSC.2008.4611652

12. **Baumgratz F.D., Saavedra C., Steyaert M., Tavernier F., Bampi S.** A wideband low noise variable-gain amplifier with a 3.4 dB NF and up to 45 dB gain tuning range in 130-nm CMOS. *IEEE Trans Circuits Syst II: Express Briefs*, 2019, Vol. 66, No. 7, Pp. 1104–1108. DOI: 10.1109/tcsii.2018.2878742

13. **Lin K., Ji L., Wei M., Chen H., Tseng J.** Design and analysis of a low noise amplifier for 5G systems. *IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW), Taichung*, 2018, Pp. 1–2. DOI: 10.1109/ICCE-China.2018.8448590

14. **Huang Z., Wang Y.** 5G wireless receiver front-end for 3.3-3.8 GHz frequency band. *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Xi'an, China, 2019, Pp. 1–4. DOI: 10.1109/EDSSC.2019.8754123

15. **Dai R., Ren J., He J., Xiao J., Kong W.** RFFE integration design for 5G in 0.13 um RFSOI technology. *China Semiconductor Technology International Conference (CSTIC)*, Shanghai, China, 2019, Pp. 1–3. DOI: 10.1109/CSTIC.2019.8755726

16. **Wong S.-K., Fabian K., Siti Maisurah Mohd Hassan, Mohd Nizam Osman, See J.H.** Design of 3 to 5 GHz CMOS low noise amplifier for ultra-wideband (UWB) system. *Progress in Electromagnetics Research C*, 2009, Vol. 9, Pp. 25–34. DOI: 10.2528/PIERC09062202

17. **Du S., Jin J., Yin H.** A low-power CMOS power amplifier for 3.1-10.6 GHz MB-OFDM ultra-wideband systems. *10th International Conference on Communication Software and Networks (ICCSN)*, Chengdu, 2018, Pp. 442–446. DOI: 10.1109/ICCSN.2018.8488311

18. **Luong G., Pham J., Medrel P., Kerhervé E.** Design of a 2.5 GHz LTE 65-nm CMOS reconfigurable power amplifier for UAV. *15th IEEE International New Circuits and Systems Conference (NEWCAS)*, Strasbourg, 2017, Pp. 253–256. DOI: 10.1109/NEWCAS.2017.8010153

19. **Santos F., Mariano A., Leite B.** 2.4 GHz CMOS digitally programmable power amplifier for power back-off operation. *IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS)*, Florianopolis, 2016, Pp. 159–162. DOI: 10.1109/LASCAS.2016.7451034

20. **Wu T., Yang J.** A multiband fully integrated high-linearity power amplifier using a 0.18-μm CMOS process for LTE applications. *International SoC Design Conference (ISOCC)*, Seoul, 2017, Pp. 31–32. DOI: 10.1109/ISOCC.2017.8368814

21. **Milićević M.M., Milinković B.S., Grujić D.N., Saranovac L.V.** Power and conjugately matched high band UWB power amplifier. *IEEE Transactions on Circuits and Systems I: Regular Papers*, Oct. 2018, Vol. 65, No. 10, Pp. 3138–3149. DOI: 10.1109/TCSI.2018.2815612

22. **Mosalam H., Allam A., Jia H., Abdel-Rahman A.B., Pokharel R.K.** High efficiency and small group delay variations 0.18-um CMOS UWB power amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, Apr. 2019, Vol. 66, No. 4, Pp. 592–596. DOI: 10.1109/TCSII.2018.2870165

23. **Ivanov M.A., Podyacheva A.A., Rumyancev I.A.** Vector modulator for 5G transceivers in 65 nm CMOS. *IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus)*, St. Petersburg, Russia, 2020, Pp. 130–133. DOI: 10.1109/EIConRus49466.2020.9039024

24. **Balashov E.V., Korotkov A.S., Rumyancev I.A.** Calibration of phase shifters on basis of vector-sum signals. *Radioelectron. Commun. Syst.*, 2018, Vol. 61, Pp. 515–521. DOI: 10.3103/S073527271811002X

25. **Zijie H., Mouthaan K.** A 0.5–6 GHz 360° vector-sum phase shifter in 0.13-μm CMOS. *IEEE MTT-S International Microwave Symposium*, Tampa, FL, 2014, Pp. 1–3. DOI: 10.1109/MWSYM.2014.6848604

26. **Huang Y.Y., Jeon H., Yoon Y., Woo W., Lee C.H., Kenney J.S.** An ultra-compact, linearly-controlled variable phase shifter designed with a novel RC poly-phase filter. *IEEE Transactions on Microwave Theory and Techniques*, Feb. 2012, Vol. 60, No. 2, Pp. 301–310. DOI: 10.1109/TMTT.2011.2177856

27. **Asoodeh A., Atarodi M.** A full 360 vector-sum phase shifter with very low RMS phase error over a wide bandwidth. *IEEE Transactions on Microwave Theory and Techniques*, June 2012, Vol. 60, No. 6, Pp. 1626–1634. DOI: 10.1109/TMTT.2012.2189227

28. **Yan T.C., Lin W.Z., Kuo C.N.** A 0.75–2.67 GHz 5-bit vector-sum phase shifter. *European Microwave Integrated Circuit Conference*, Nuremberg, 2013, Pp. 196–199.

29. **Zheng Y., Saavedra C.E.** Full 360 vector-sum phase-shifter for microwave system applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, Apr. 2010, Vol. 57, No. 4, Pp. 752–758. DOI: 10.1109/TCSI.2009.2025851

30. **Balashov E.V., Rumyancev I.A.** A fully integrated 6-bit vector-sum phase shifter in 0.18 um CMOS. *Proc. of the 11th International Siberian Conference on Control and Communications*, 21-23 May 2015, Omsk, Russia, Pp. 1–5. DOI: 10.1109/SIBCON.2015.7146991

31. **Balashov E.V., Korotkov A.S., Rumyancev I.A.** An unbalanced transformerless vector-sum phase shifter in 0.18 μm CMOS problems of advanced micro- and nanoelectronic systems development. *Selected Articles of VII All-Russia Science & Technology Conference MES-2016*, Part III. Moscow, IPPM RAS, 2017, Pp. 2–5.

Received 19.12.2020.

СПИСОК ЛИТЕРАТУРЫ

1. 5G Spectrum Public Policy Position // URL: http://www-file.huawei.com/-/media/corporate/pdf/public-policy/public_policy_position_5g_spectrum.pdf (Дата обращения: 02.02.2021).

2. 5G Spectrum GSMA Public Policy Position // URL: https://www.gsma.com/spectrum/wp-content/uploads/2020/03/5G-Spectrum-Positions.pdf (Дата обращения: 02.02.2021).

3. Выделены полосы для создания пилотных зон сетей связи 5G // URL: https://digital.gov.ru/ru/events/38690/ (Дата обращения: 02.02.2021). (rus)

4. **Rumyancev I.A., Korotkov A.S.** Survey on beamforming techniques and integrated circuits for 5G systems // IEEE Internat. Conf. on Electrical Engineering and Photonics. St. Petersburg, Russia, 2019. Pp. 76–80. DOI: 10.1109/EExPolytech.2019.8906842

5. **Peterson B., Schnaufer D.** 5G fixed wireless access array and RF front-end trade-offs // Microwave Journal. 14 Feb. 2018. Pp. 1-9.

6. **Pilipko M.M., Manokhin M.E.** Design of a low-power 12-bit SAR ADC // IEEE Conf. of Russian Young Researchers in Electrical and Electronic Engineering. St. Petersburg, Russia, 2019. Pp. 129–131. DOI: 10.1109/EIConRus.2019.8657039

7. **Budanov D.O., Morozov D.V., Pilipko M.M.** An 8-bit analog-to-digital converter with a novel encoder using 90 nm CMOS // IEEE Internat. Conf. on Electrical Engineering and Photonics. St. Petersburg, 2018. Pp. 56–59. DOI: 10.1109/EExPolytech.2018.8564441

8. **Enuchenko M.S., Morozov D.V., Pilipko M.M.** An 8-bit parallel DAC with segmented architecture // J. Commun. Technol. Electron. 2017. No. 62. Pp. 89–100. DOI: 10.1134/S1064226917010053

9. **Stesev G., Budanov D., Balashov E.** Serial-to-parallel converter using GaAs D-Mode transistors // IEEE Internat. Conf. on Electrical Engineering and Photonics. St. Petersburg, Russia, 2020. Pp. 67–70. DOI: 10.1109/EExPolytech50912.2020.9243862

10. **Балашов Е.В., Коротков А.С.** Микроэлектронные малошумящие КМОП-усилители радиочастотного диапазона: применение, схемотехника, тенденции развития // Успехи современной радиоэлектроники. 2007. № 2. С. 3–34.

11. **Balashov E.V., Korotkov A.S.** Ultra wideband low noise amplifier with source degeneration and shunt series feedback // 4th European Conf. on Circuits and Systems for Communications, Bucharest, Romania. 2008. Pp. 87–92. DOI: 10.1109/ECCSC.2008.4611652

12. **Baumgratz F.D., Saavedra C., Steyaert M., Tavernier F., Bampi S.** A wideband low noise variable-gain amplifier with a 3.4 dB NF and up to 45 dB gain tuning range in 130-nm CMOS // IEEE Trans Circuits Syst II: Express Briefs. 2019. Vol. 66. No. 7. Pp. 1104–1108. DOI: 10.1109/tcsii.2018.2878742

13. **Lin K., Ji L., Wei M., Chen H., Tseng J.** Design and analysis of a low noise amplifier for 5G systems // IEEE Internat. Conf. on Consumer Electronics-Taiwan (ICCE-TW). Taichung, 2018. Pp. 1–2. DOI: 10.1109/ICCE-China.2018.8448590

14. **Huang Z., Wang Y.** 5G wireless receiver front-end for 3.3-3.8 GHz frequency band // IEEE Internat. Conf. on Electron Devices and Solid-State Circuits. Xi'an, China, 2019. Pp. 1–4. DOI: 10.1109/EDSSC.2019.8754123

15. **Dai R., Ren J., He J., Xiao J., Kong W.** RFFE integration design for 5G in 0.13 um RFSOI technology // China Semiconductor Technology Internat. Conf. (CSTIC). Shanghai, China, 2019. Pp. 1–3. DOI: 10.1109/CSTIC.2019.8755726

16. **Wong S.-K., Fabian K., Siti Maisurah Mohd Hassan, Mohd Nizam Osman, See J.H.** Design of 3 to 5 GHz CMOS low noise amplifier for ultra-wideband (UWB) system // Progress in Electromagnetics Research C. 2009. Vol. 9. Pp. 25–34. DOI: 10.2528/PIERC09062202

17. **Du S., Jin J., Yin H.** A low-power CMOS power amplifier for 3.1-10.6 GHz MB-OFDM ultra-wideband systems // 10th Internat. Conf. on Communication Software and Networks. Chengdu, 2018. Pp. 442–446. DOI: 10.1109/ICCSN.2018.8488311

18. **Luong G., Pham J., Medrel P., Kerhervé E.** Design of a 2.5 GHz LTE 65-nm CMOS reconfigurable power amplifier for UAV // 15th IEEE Internat. New Circuits and Systems Conf. Strasbourg, 2017. Pp. 253–256. DOI: 10.1109/NEWCAS.2017.8010153

19. **Santos F., Mariano A., Leite B.** 2.4 GHz CMOS digitally programmable power amplifier for power back-off operation // IEEE 7th Latin American Symp. on Circuits & Systems. Florianopolis, 2016. Pp. 159–162. DOI: 10.1109/LASCAS.2016.7451034

20. **Wu T., Yang J.** A multiband fully integrated high-linearity power amplifier using a 0.18-μm CMOS process for LTE applications // Internat. SoC Design Conf. Seoul, 2017. Pp. 31–32. DOI: 10.1109/ISOCC.2017.8368814

21. **Milićević M.M., Milinković B.S., Grujić D.N., Saranovac L.V.** Power and conjugately matched high band UWB power amplifier // IEEE Transactions on Circuits and Systems I: Regular Papers. Oct. 2018. Vol. 65. No. 10. Pp. 3138–3149. DOI: 10.1109/TCSI.2018.2815612

22. **Mosalam H., Allam A., Jia H., Abdel-Rahman A.B., Pokharel R.K.** High efficiency and small group delay variations 0.18-um CMOS UWB power amplifier // IEEE Transactions on Circuits and Systems II: Express Briefs. Apr. 2019. Vol. 66. No. 4. Pp. 592–596. DOI: 10.1109/TCSII.2018.2870165

23. **Ivanov M.A., Podyacheva A.A., Rumyancev I.A.** Vector modulator for 5G transceivers in 65 nm CMOS // IEEE Conf. of Russian Young Researchers in Electrical and Electronic Engineering. St. Petersburg, Russia, 2020. Pp. 130–133. DOI: 10.1109/EIConRus49466.2020.9039024

24. **Balashov E.V., Korotkov A.S., Rumyancev I.A.** Calibration of phase shifters on basis of vector-sum signals // Radioelectron. Commun. Syst. 2018. Vol. 61. Pp. 515–521. DOI: 10.3103/S073527271811002X

25. **Zijie H., Mouthaan K.** A 0.5–6 GHz 360° vector-sum phase shifter in 0.13-μm CMOS // IEEE MTT-S Internat. Microwave Symp. Tampa, FL, 2014. Pp. 1–3. DOI: 10.1109/MWSYM.2014.6848604

26. **Huang Y.Y., Jeon H., Yoon Y., Woo W., Lee C.H., Kenney J.S.** An ultra-compact, linearly-controlled variable phase shifter designed with a novel RC poly-phase filter // IEEE Transactions on Microwave Theory and Techniques. Feb. 2012. Vol. 60. No. 2. Pp. 301–310. DOI: 10.1109/TMTT.2011.2177856

27. **Asoodeh A., Atarodi M.** A full 360 vector-sum phase shifter with very low RMS phase error over a wide bandwidth // IEEE Transactions on Microwave Theory and Techniques. June 2012. Vol. 60. No. 6. Pp. 1626–1634. DOI: 10.1109/TMTT.2012.2189227

28. **Yan T.C., Lin W.Z., Kuo C.N.** A 0.75–2.67 GHz 5-bit vector-sum phase shifter // European Microwave Integrated Circuit Conf. Nuremberg, 2013. Pp. 196–199.

29. **Zheng Y., Saavedra C.E.** Full 360 vector-sum phase-shifter for microwave system applications // IEEE Transactions on Circuits and Systems I: Regular Papers. Apr. 2010. Vol. 57. No. 4. Pp. 752–758. DOI: 10.1109/TCSI.2009.2025851

30. **Balashov E.V., Rumyancev I.A.** A fully integrated 6-bit vector-sum phase shifter in 0.18 um CMOS // Proc. of the 11th Internat. Siberian Conf. on Control and Communications. Omsk, Russia, May 2015. Pp. 1–5. DOI: 10.1109/SIBCON.2015.7146991

31. **Balashov E.V., Korotkov A.S., Rumyancev I.A.** An unbalanced transformerless vector-sum phase shifter in 0.18 μm CMOS problems of advanced micro- and nanoelectronic systems development // Selected Articles of VII All-Russia Science & Technology Conf. MES-2016. Part III. Moscow: IPPM RAS, 2017. Pp. 2–5.

Статья поступила в редакцию 19.12.2020.

THE AUTHOR / СВЕДЕНИЯ ОБ АВТОРЕ

Rumyancev Ivan A.
Румянцев Иван Александрович
E-mail: i.a.rumiantsev@spbstu.ru