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CMOS INDUCTOR DESIGN FEATURES FOR LTE DEVICES

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This work is devoted to some aspects of the development of planar elements of the microwave path, which are used in the design of low-noise LTE range amplifiers, namely inductors, for further employment as part of the NB-IoT transceiver. General theoretical calculations on the design of high-frequency inductors are given. By the example of a multilayer CMOS 90 nm inductor with a nominal value of 7 nH, we demonstrated the influence of the structure thickness obtained by replicating layers used to get the required skin layer thickness and to achieve the best quality factor in the LTE frequency range from 0.5 to 3.5 GHz by means of electromagnetic (EM) models. For a better understanding of the inductor operation, the models obtained as a result of the EM simulation for different values of the substrate conductivity are compared. The obtained data partially refute the need of increasing the maximum thickness of the inductors by a set of upper metals combined using multiple TSV arrays for silicon process stacks. Due to the increasing of the capacitive influence of the substrate on the lower metal layers of the inductor, the highest values of Q-factor and self-resonance frequencies are achieved by the structures with a minimum number of metal layers, despite the negative influence of the skin effect for low frequencies.

Keywords: LTE, NB-IoT, inductance coil, 3D inductor, CMOS, EM analysis.

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ОСОБЕННОСТИ ПРОЕКТИРОВАНИЯ КМОП КАТУШЕК ИНДУКТИВНОСТИ ДЛЯ УСТРОЙСТВ LTE ДИАПАЗОНОВ ЧАСТОТ

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Статья посвящена некоторым аспектам разработки планарных элементов СВЧ-тракта, которые используются при проектировании малошумящих усилителей LTE диапазона, а именно катушкам индуктивности, для дальнейшего применения в составе приемопередатчика NB-IoT. Даны общие теоретические выкладки по проектированию высокочастот-

ных катушек индуктивности. На примере многослойной КМОП 90 нм катушки номиналом 7 нГн, при помощи электромагнитных (ЭМ) моделей, продемонстрировано влияние толщины структуры, полученной при помощи реплицирования слоев, для набора требуемой толщины скин-слоя и достижения наилучших показателей добротности в частотном диапазоне LTE от 0,5 до 3,5 ГГц. Для наиболее полного представления о работе катушки проведено сравнение моделей, полученных в результате ЭМ симуляции для разных значений проводимости подложки. Полученные данные частично опровергают необходимость наращивания максимальных толщин интегральных катушек индуктивности путем набора верхних металлов, объединенных при помощи множественных массивов TSV, для стеков кремниевых процессов. Из-за увеличения емкостного влияния подложки по отношению к нижним слоям металлизации катушки индуктивности, наибольшие значения добротности и частот собственного резонанса достигаются на конструкциях с минимальным числом слоев металлизации вопреки негативному влиянию скин-эффекта для малых частот.

Ключевые слова: LTE, NB-IoT, катушка индуктивности, 3D-индуктор, КМОП, ЭМ анализ.

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Introduction

The rapid growth of the telecommunications industry under the auspices of the announced 5G (and 6G in the future) communication networks has led to the new frequency bands development. At the same time, within the already known frequency ranges, new communication standards and protocols are emerging, forming new areas of application of microelectronic devices in telecommunication systems, such as the Internet-of-Things represented in 3GPP: LTE-M, EC-GSM-IoT, NB-IoT [1] for example.

To provide a competitive position in the mass segment of the telecommunications market, the proposed device must be cheap and technologically advanced. Currently, when designing integrated circuits (IC) for telecommunications, the most widely used silicon technologies are CMOS and SiGe [2], which allow us to provide the required parameters of the element base [3]. At a relatively low cost, silicon technologies allow the implementation of both digital and analog system nodes and systems for the “mixed signals” processing.

This work is devoted to some aspects of RFIC passive planar elements design used in the low-noise amplifiers of the LTE frequency bands range, namely inductance coils or inductors.

Figure 1 shows a functional diagram of a proposed NB-IoT transceiver. A homodyne receiver is used as a receiver.

The building blocks of the receiving (RX) channel of the transceiver device include a bandpass filter of the preselector (BPF), a low-noise amplifier (LNA), a quadrature demodulator (based on mixers with a shift of 90 degrees), automatic gain control systems (AGC-VGA) and low-pass filters (LPF). The LNA is one of the key circuit nodes. In terms of signal conversion and processing, the LNA is responsible for the sensitivity of the receiver and its dynamic range.

The transmitting (TX) channel consists of low-pass filters (LPF), buffer amplifiers (BA), a quadrature modulator, a high-frequency amplifier (HFA), a bandpass filter (BPF), and a power amplifier (PA). As shown in the Fig. 1, the antenna bandpass filters of the receiver and transmitter, and the PA_{TX} are discrete, while the rest of the elements are integrated.

Depending on the type of transceiver (for broadband devices or devices with multiple operating ranges), the LNA can determine the receiver bandwidth by providing uniform gain flatness over the operating range and reverse loss values. Another important thing is that in the transceiver RX channel (usually for communication systems), the LNA [4] is the first device that interacts with the antenna. As the result, the LNA input impedance is a required to match the antenna and minimize insertion loss and distortion.

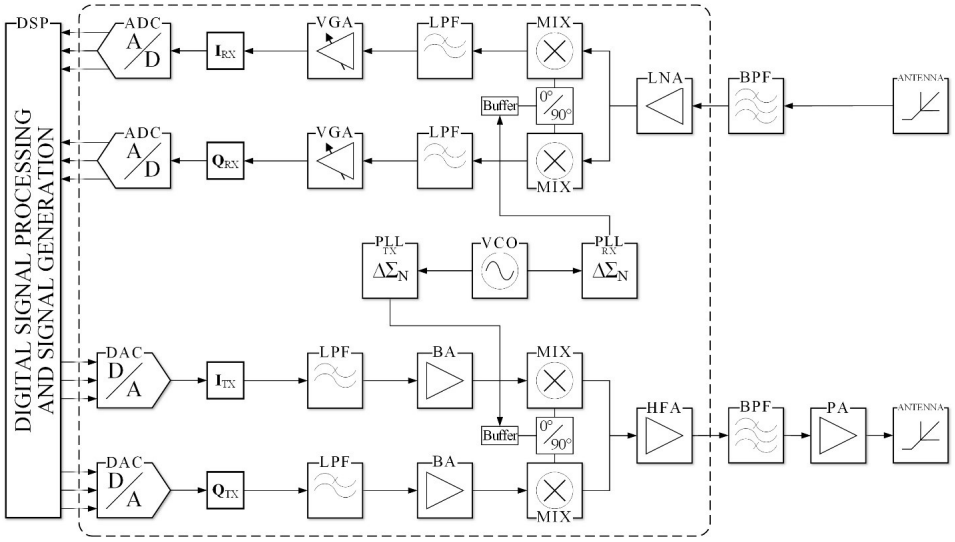


Fig. 1. Functional diagram of the NB-IoT transceiver

One of the simplest ways to design a low noise amplifier is a cascode amplifier circuit. Works [5–7] present the calculated data of the noise figure and the gain of the cascoded LNA models in the frequency domain depending on the various parameters of the inductor – the quality factor and the nominal inductance. These dependencies clearly illustrate the contribution of the coil to the final parameters of the LNA device. Thus, one of the fundamental tasks is to ensure the maximum Q-factor of the inductor cell. Another one is to ensure the required level of the quality factor throughout the entire operating frequency range [8]. These tasks are familiar to all developers of inductors and capacitors, regardless of their design (integral or lumped), but silicon processes introduce some specifics into the development of these elements.

Research and design of RF multilayer inductors

The equations calculating the inductance of flat planar inductors (1, 2 – example for octagonal inductance coil) were formulated by Greenhouse [9, 10] more than 40 years ago and are relevant to date:

$$L = \frac{\mu n^2 d_{avg} C_1}{2}\left(\ln\left(\frac{C_2}{\rho}\right) + C_3\rho + C_4\rho^2\right), \quad (1)$$

$$L = \frac{1.07\mu n^2 d_{avg}}{2}\left(\ln\left(\frac{2.29}{\rho}\right) + 0.19\rho^2\right), \quad (2)$$

where $C_1 ... C_4$ are layout dependent coefficients from Table 1 (based on face spiral number), n is the number of turns, μ is conductor permeability, d_{avg} is the average diameter determined as $d_{avg} = 0.5(d_{OUT} + d_{IN})$, ρ is special outer versus inner diameter ratio, which is determined as $\rho = (d_{OUT} - d_{IN})/(d_{OUT} + d_{IN})$.

The integrated resonant structures are used as RLC models (Fig. 2*a*), as well as their adaptations for high-frequency circuits, "π-models" (pi-models) [11] (Fig. 2*b*), which describe inductors using the coefficients of admittance matrices.

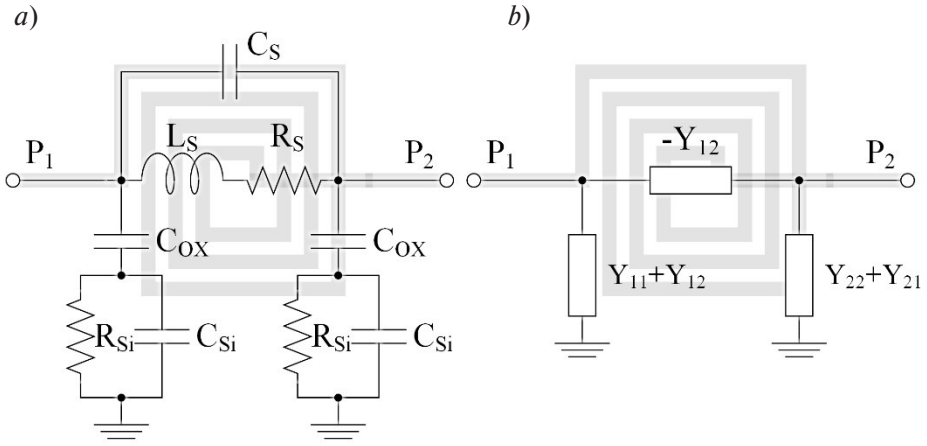


Fig. 2. IC inductor: *a* – lumped circuit; *b* – pi-model

Table 1

Spiral inductor layout coefficients

Layout	C_1	C_2	C_3	C_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

The equations for calculating the quality factor (Q) and inductance (L) are presented below (3, 4):

$$L = \frac{Im\left(\frac{1}{Y_{11}}\right)}{\omega} = \frac{Im\left(\frac{1}{Y_{11}}\right)}{2\pi f}, \tag{3}$$

$$Q = \frac{Im\left(\frac{1}{Y_{11}}\right)}{Re\left(\frac{1}{Y_{11}}\right)} = -\left(\frac{Im(Y_{11})}{Re(Y_{11})}\right), \tag{4}$$

where Y_{11} is the input admittance from Y-parameter matrix, ω is the angular frequency given by $\omega = 2\pi f$, $Re(X)$ and $Im(X)$ are the real and imaginary parts of the complex value X in the parentheses.

While developing integrated inductors and capacitors based on Si CMOS and SiGe BiCMOS technologies, the designer faces some fundamental problems. The first one is the thickness of the skin layer [12, 13], which determines the depth of alternating current flow in the conductor surface, depending on the thickness and material of the conductor. Silicon processes in general are characterized by a large number (6 or more) of metal layers with small thickness (usually less than 1 micron). Some factories provide special options (so-called RF options) that expand the number of metallization layers by adding one or more up-

per layers of "thick metals" with thicknesses of 1 μm or more. Without these additions, the developer may face difficulties when designing devices in the sub-GHz domain [14]. At frequencies of about 500 MHz (typical for the lower bands of the LTE standard), the thickness of the skin layer is about 3.5 microns which will directly affect the quality factor of the entire structure. Unable to achieve the required thickness in the upper stack of metallization layers, the developers use the replication of the inductor layers [15] in several metal layers located below. These layers are connected with arrays of transition holes (through-silicon vias – TSV arrays), like a solid metal layer conductor, thereby increasing the thickness to the desired values.

The second problem is the proximity of the self-resonant frequency (SRF) – the point in the frequency domain that marks the transition from the inductive to the capacitive region of the impedance (or capacitive to inductive in the case of a capacitor design). When approaching the frequency of self resonance, the inductance of the RF inductor begins to grow to a peak value, after which there is a sharp fall in the characteristic and a transition to the opposite impedance region. The higher the value of the inductor, the more difficult it is to achieve high self-resonance frequencies. In some cases, designers can increase the SRF frequency by using special patterns of slotted screens (patterned ground shield, PGS) [16] to "tune" the magnetic field of the inductor.

In this work, it is proposed to consider a model of a symmetrical inductor. Geometry and area are calculated in advance using variations of the parameters mentioned in the formulas above (1, 2). Table 2 presents a diagram of the topology and main parameters of the inductor.

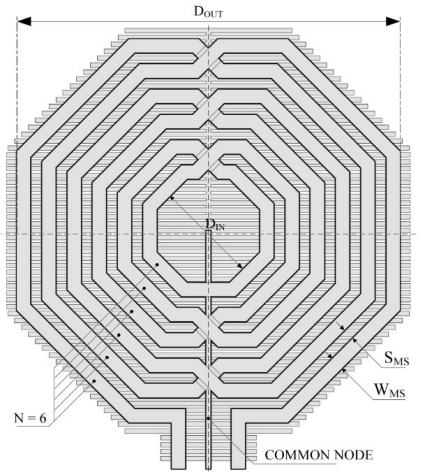
To overcome the negative effects caused by the skin-depth at low frequencies, we used a repetition of several upper metal layers with TSV / via-arrays. Such a constructive solution should allow reaching the maximum Q-factor values for a given inductor structure within a common 90 nm CMOS process. The operating frequency range of the device, in which the inductor cell is supposed to be used, is determined by the frequency bands of the NB-IoT transmitter operating in the LTE frequency range.

The specified working bandwidth of the inductor lies within 0.5 ... 3.5 GHz, therefore the most significant parameters (L, Q) must correspond to the calculated values over the entire operating range.

Computer EM simulation using the extraction of electromagnetic parameters is an extremely costly operation, depending on the required time and the workstation calculating power. To optimize the development process, approximations of via-arrays (thousands of individual holes were replaced by solid polygons) and cell boundary conditions (protective ring elements were replaced by ideal conductors at plane boundaries) were used.

Table 2

The main planar parameters of the inductor



Parameter	Designation	Value
Number of turns	N	6
Microstrip width, um	W_{MS}	12
Microstrip spacing, μm	S_{MS}	10
Outer diameter, μm	D_{OUT}	334
Inner diameter, μm	D_{IN}	90
Calculated inductance value, nH	L	6.9 ... 7.2

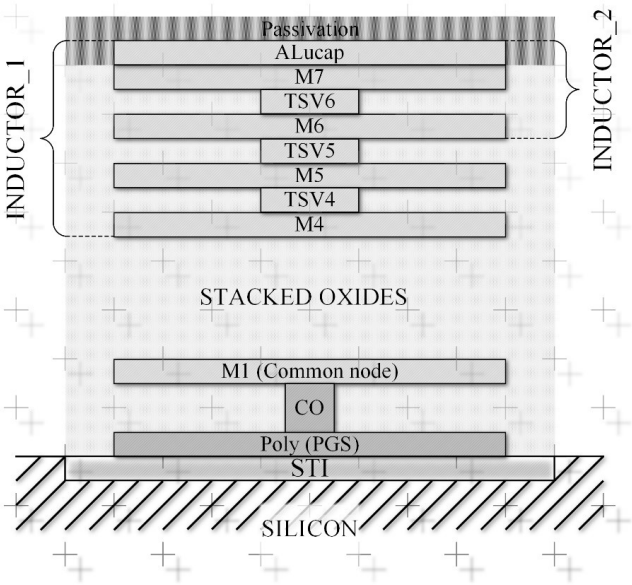


Fig. 3. Layer stack profile of the inductor based on CMOS 90 nm technology

As a computer research, it is proposed to simulate and compare the inductor with different metallization thicknesses due to the different compositions of the layers involved in the structure (Fig. 3). This approach gives a qualitative idea of the parameters of the inductor at metallization thicknesses of ≈4.63 microns for "Inductor_1" and ≈2.1 microns for "Inductor_2".

In addition, EM simulation was carried out on different silicon substrates based on different conductivities of Si-substrate: high-resistance (HR) and low-resistance (LR) silicon. The finite element method (FEM) was used as a mathematical solver mechanic.

The computer modeling results form S-parameters data extraction using Eqs. 3 and 4 presented in Fig. 4, 5 and 6 show the following matrices: the initial matrix of S-parameters obtained as a result of EM analysis and the matrix of Y-parameters derived from the initial S-parameters.

The triangular marker indicates the characteristics of the inductance coil with a large number of metal layers (Fig. 3, Inductor_1), and, accordingly, the round marker is attached to the thin structure (Inductor_2). Different types of lines indicate results for substrates with different conductivity values: continuous for low resistance (LR) and dashed for high resistance (HR) values. A marker with a square denotes the model parameters based on SPICE simulation for a structure with a large number of layers (Inductor_1). It should be noted that the analysis of small-sized structures using the FEM is time-consuming and extremely demanding on the workstation computing power, especially on the RAM.

Figure 4 shows the S- and Y-parameters on the Smith chart of complex characteristics. The S-parameters on the left give an idea of the consistency of all the structures presented. It is shown that upon approaching the mutual resonance frequencies and after them, the structures are mismatched. In the Y diagram (admittance parameters), we can observe that the structures have a clearly defined "inductive" behavior range and that they are ideally symmetrical (superimposed on each other and completely repeated) concerning the first and second ports, i.e. Y (1,1) = Y (2,2). Thus, given the symmetry, there is no need to further consider the characteristics of the conductivities Y (1,1) and Y (2,2) for both ports.

A graph (Fig. 5) shows the frequency dependence of the reactance to the angular frequency, with inductance from Eq. (3), for all the structures under consideration. All the presented variants of inductors have a similar inductance pattern up to 2 GHz, corresponding to ≈7 nH (determined by the geometry of the Table 2), after which, due to the proximity of the SRF, a sharp rise in the characteristic occurs, followed by a fall and transition to the capacitive reactance hemisphere.

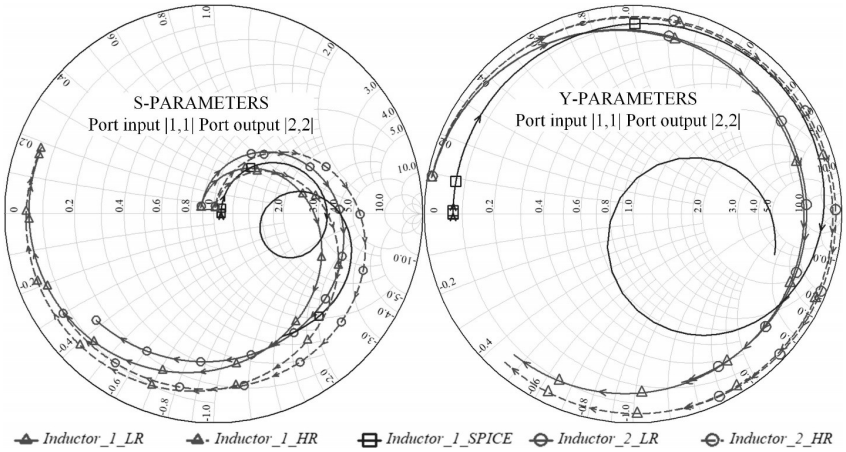


Fig. 4. Smith charts: S-parameters (left) and Y-parameters (right)

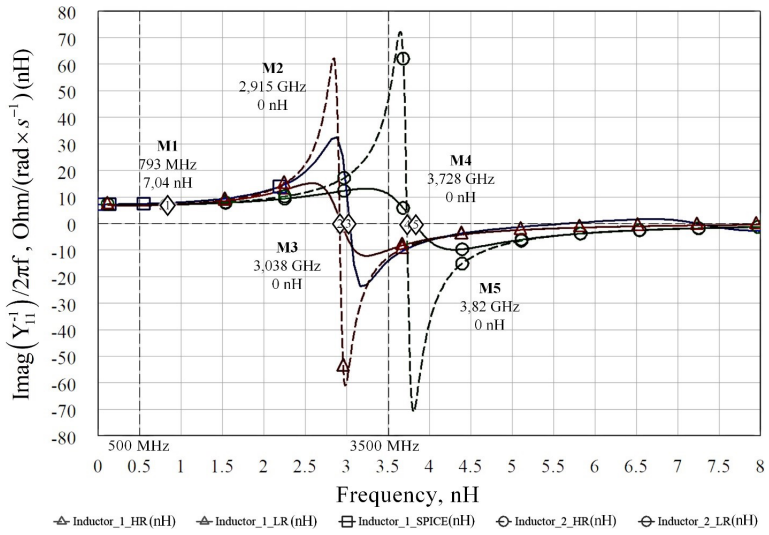


Fig. 5. Frequency dependence of the reactance to the angular frequency (inductance)

Figure 5 shows that the structure with a smaller number of metal layers has high SRF value, while "Inductor_1" has a cutoff of the operating band due to the presence of self-resonance frequencies at ≈2.915 GHz for model simulations with different substrates (HR and LR).

In addition, the frequency dependence of the "Inductor_1" structure with the number of upper metals equal to 7 correlates with the data obtained from the result of SPICE modeling in the range of self-resonance frequencies, which indicates the correctness of the model and development methodology of this device. The difference in peak amplitudes in this case is not so significant and is explained by the difference in the conductivity of the substrate.

Figure 6 illustrates Q-factor versus frequency with coil conductor thicknesses dependence from Eq. (4). According to the model, the Q-factor for a low-resistance substrate does not significantly differ when switching from a three-layer to a five-layer inductor topology, while the thin structure has a high Q-factor characteristic due to the delayed mutual resonance frequency (Fig. 5). The difference becomes much more significant when using a high-resistance (HR) substrate. The Q-factor obviously increases almost twice as much in both structures, while given the removal of the SRF, the thin structure "Inductor_2" has a flatter characteristic along with the operating frequency band (0.5 ... 3.5 GHz) with a higher amplitude of up to 18.03. The SPICE model values for the first inductor generally correlate with the absolute

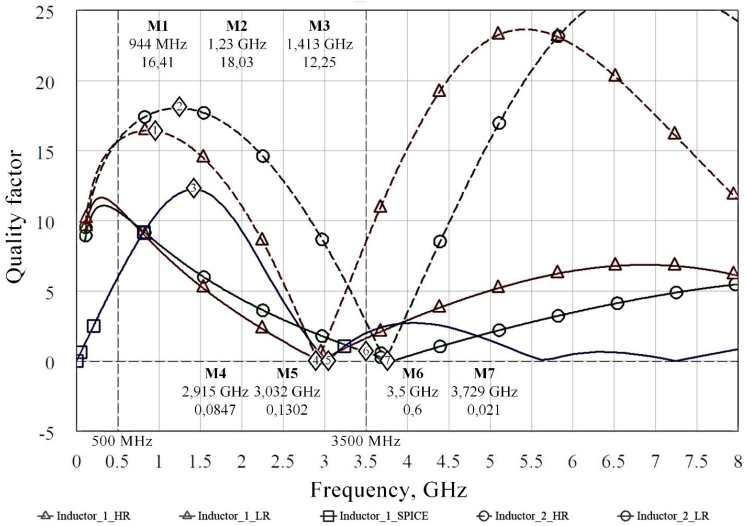


Fig. 6. Quality factor in the frequency domain

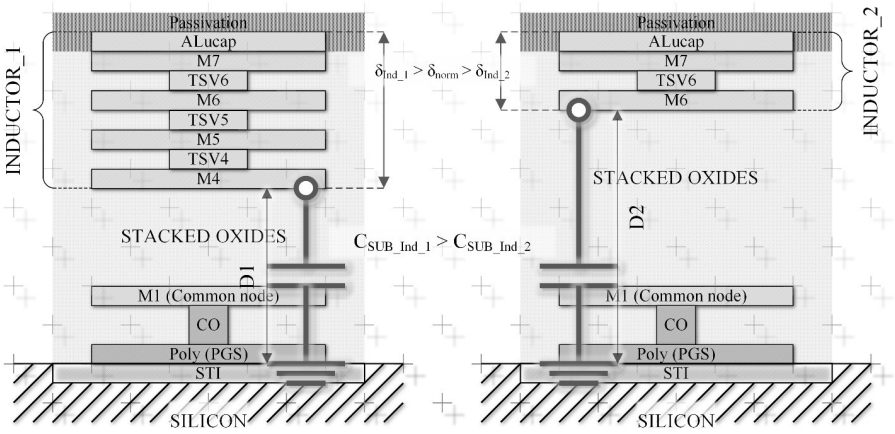


Fig. 7. Inductor models comparison

Q values obtained on the LR substrate but are shifted at the peak towards the low frequencies. In contrast to the results obtained from the EM model, the SPICE model has several self-resonance frequencies outside the operating range in the surveyed area, which explains the difference in Q after the first self-resonance frequency (3.038 GHz).

The results summary of the inductor models using EM FEM simulations is presented in Table 3.

Table 3

Inductor simulation results

Designation	Low resistance substrate (LR)				High resistance substrate (HR)			
	Inductor_1		Inductor_2		Inductor_1		Inductor_2	
Structure thickness (T), μm	4.63		2.1		4.63		2.1	
Frequency (F), GHz	0.5	3.5	0.5	3.5	0.5	3.5	0.5	3.5
Inductance (L), nH	6.81	–	7.01	11.6	6.87	–	7.01	46.57
Quality factor (Q)	10.96	–	10.69	0.63	15.68	–	15.75	2.79

Conclusion

Based on the simulation results, it can be concluded that "Inductor_2" exhibits better parameters in the frequency range with a smaller thickness, and this is despite the fact that at frequencies of about 500 MHz, large skin layer thickness (~3.5 μm) is required. This effect is caused by the fact that the capacitance of the inductor (Fig. 7) to the substrate increases sharply with the use of more metal layers, and, conversely, for a thin inductance coil, the capacitive coupling drops so much that it exceeds the negative effect caused by the thickness of the skin layer.

The use of a high resistance silicon substrate (HR) gives a significant increase in figure of merit in relation to structures based on low resistance (LR) silicon substrates. In this case, the frequencies of the self-resonance point and the point of minimum values of the figure of merit do not strongly depend on the conductivity of the substrate.

Thus, the replication of the inductor layers to the maximum metallization thicknesses in silicon processes can lead to a deterioration in the frequency properties of the device when operating in the LTE bands. A complete picture of coil behavior requires finite element EM modeling.

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