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## MODELING THE IMPACT OF TECHNOLOGICAL PROCESS VARIATIONS ON R-2R DAC STATIC CHARACTERISTICS

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Digital-to-analog converter (DAC) is widely used in modern integrated electronics, converting digital signals into analog ones. This paper considers an R-2R structure DAC, its operation principle and static characteristics: integral non-linearity (INL) and differential non-linearity (DNL). For the accuracy of this DAC conversion, it is important that the element resistance ratio is maintained for the entire circuit. The authors considered the influence of random and systematic errors of DAC elements resistances on the transfer function and static characteristics of DAC, as well as the use of special DAC element placements to compensate for systematic errors. Systematic errors are presented as three types of gradients: linear, quadratic and central quadratic. These gradients were modeled in MATLAB. Using the MATLAB script, the authors calculated the static characteristics of the R-2R DAC for two resistor placements: regular and common centroid, taking into account the impact of three different gradients. These placements were compared based on the modeling and calculation results.

**Keywords:** digital-analog conversion, R-2R, linear gradient, quadratic gradient, resistor mismatch, MATLAB, common centroid.

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## МОДЕЛИРОВАНИЕ ВОЗДЕЙСТВИЯ ТЕХНОЛОГИЧЕСКОГО РАЗБРОСА НОМИНАЛОВ ЭЛЕМЕНТОВ НА СТАТИЧЕСКИЕ ХАРАКТЕРИСТИКИ ЦАП ТИПА R-2R

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ЦАП широко используются в современной интегральной электронике, осуществляя преобразование цифрового сигнала в аналоговый. В статье рассматривается ЦАП структуры R-2R, его принцип работы и статические характеристики: интегральная нелинейность (INL) и дифференциальная нелинейность (DNL). Для точности преобразования данного ЦАП важно, чтобы соотношение сопротивлений элементов сохранялось для всей схемы. Изучено влияние случайных и систематических погрешностей

номиналов резисторов на выходную и статические характеристики ЦАП, а также использование специальных расстановок элементов ЦАП для компенсации систематических погрешностей. Систематические ошибки представлены в виде трех типов градиентов: линейного, квадратичного и центрального квадратичного. Выполнено моделирование данных градиентов в MATLAB. С помощью скрипта MATLAB сделан расчет статических характеристик ЦАП R-2R с учетом воздействия трех различных градиентов при двух расстановках резисторов: «обычная» и «с общим центром». По результатам моделирования и расчета выполнено сравнение данных расстановок.

**Ключевые слова:** цифро-аналоговый преобразователь, R-2R, линейный градиент, квадратичный градиент, MATLAB, расстановка с общим центром.

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### Introduction

Digital-to-analog converters (DAC) are widely used in modern complex mixed-signal integrated circuits, performing a conversion of a digital signal into an analog one. There are various types of DACs, which convert input signals with different resolutions into the output analog voltage or current. All digital-to-analog converters can be divided into the two main groups: serial and parallel DACs [1].

A DAC based on resistive matrix R-2R belongs to the parallel DACs of the binary architecture, since the output signal is formed by summing the voltages from the switched weighting elements [2]. In general, the weighting elements are resistances and, according to the weighting method, they are formed as a resistive ladder [1]. The schematic of an ideal 8-bit R-2R DAC is shown in Fig. 1.

As a rule, DAC converts an input signal from the digital binary code to the output continuous voltage. The output analog signal formed as a sum of the voltages at the DAC inputs is multiplied by the appropriate weighting coefficients. In the ideal case, when manufacturing DACs, there is no weight element ratio error, so the resistor ratios from the R-2R ladder are precisely matched and the DAC weights can be  $2^{-(N-i+1)}$ , where “N” is the DAC resolution, “i” is the bit number [3]. In reality, there are always random and systematic errors due to imperfectly matched resistors from the R-2R ladder [4]. To minimize DAC conversion error, it is necessary to maintain a certain ratio between R and 2R resistances [5–6].

Random errors are the component (e.g. weighting components – resistors) errors that occur during chip production. They can be calculated within the normal distribution with the manufacturer’s specified variation. Systematic errors are the errors caused by external factors affecting all weighting elements simultaneously and depending on the placement of each element on the chip [7].

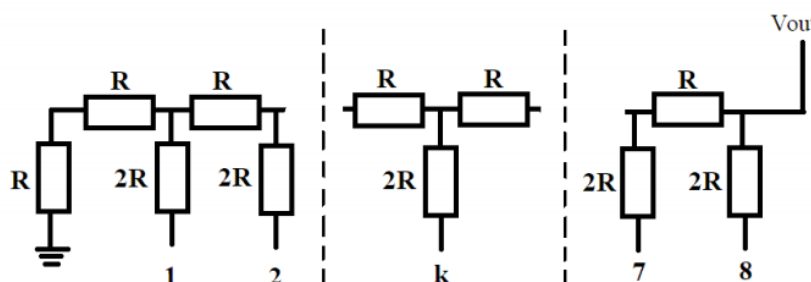


Fig. 1. Schematic of an ideal R-2R DAC based on a resistive ladder

### The problem of systematic errors

In this paper, we will consider systematic errors affecting R-2R resistances. To reduce random errors, geometric dimensions of the weighting components can be increased [8–10]. Therefore, random errors become insignificant and the impact of systematic errors increases. Thus, the impact of a systematic error typically prevails over that of a random error.

Under certain assumptions, systematic errors can be represented with some accuracy in the form of a linear or quadratic gradient [11–13] describing the deviation of the weight elements (resistances) placed on a chip. In order to solve the problem of the negative impact of these gradients, which leads to increased DAC integral and differential non-linearities, designers widely use gradient-compensated placement for the weighting elements where gradient is compensated and the matched resistance ratio for all elements is preserved [14].

On the one hand, the optimal placement of DAC array elements in terms of minimizing the area occupied on the chip and the absence of parasitic capacitances implies simplification of the connection and reduction of parasitic capacitances [1]. However, this placement can be susceptible to various systematic errors which have a negative impact on DAC characteristics [15].

### Simulation by MATLAB script

In order to find a compromise between gradient compensation and connection simplification, it is necessary to evaluate DAC characteristics (in particular, integral and differential non-linearity) for the given placement of the weighting elements (resistors). The MATLAB script used in this paper can simulate horizontal and vertical gradients on the weighting elements placed on the chip. The script allows to model three types of the gradient: linear, quadratic and central quadratic (Fig. 2).

The script also calculates the actual weighting coefficients and the DAC transfer characteristic taking into account the non-idealities of the resistance values. The R-2R array element placement is formed as a number matrix with the element numeration strictly ordered as shown in Fig. 3. The proposed script is

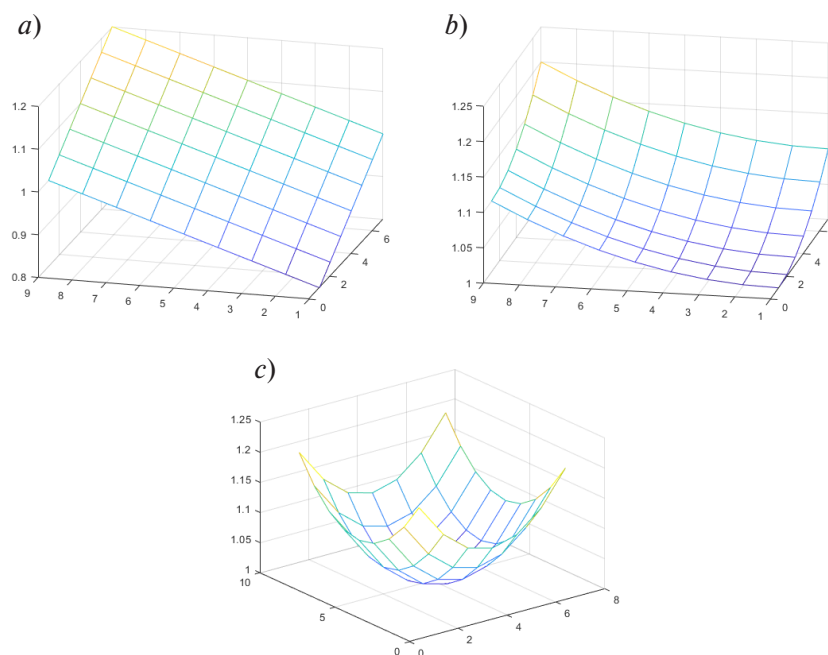


Fig. 2. The gradient map simulation: *a* – linear; *b* – quadratic; *c* – central quadratic

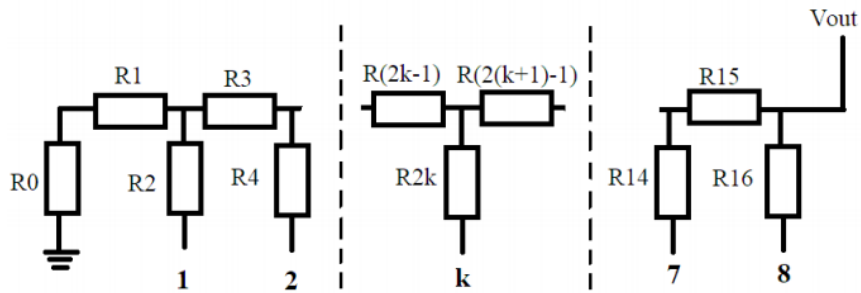


Fig. 3. R-2R weighting elements

suitable for any number of the weighting elements on a chip, as well as for any DAC resolution; the calculation of integral nonlinearity (INL) and differential nonlinearity (DNL) is also included in the MATLAB script.

Comparison of the various ways of placing R-2R array elements on a chip is studied and static DAC characteristics are evaluated (in particular, INL and DNL) for a given type of gradient and the placement of DAC weighting elements on the chip. The script produces the following graphs:

1. Transfer characteristic – relationship between the value of the output voltage  $V_{out}$  and the given DAC input code.
2. DNL – deviation of an output step from the ideal analog LSB value scaled to the value of conversion step (LSB).
3. INL – deviation of the actual transfer characteristic from the ideal transfer curve for each output level scaled to the value of conversion step (LSB) [16].

### Comparison of two placements

In this paper, we consider two choices for the placement of the 8-bit DAC weighting elements: with a common center (“common-centroid”) and without compensation for distortion (“regular”). The first one was designed to achieve full compensation of the linear gradient and the second one was chosen as the simplest in terms of connections and the area on the chip.

The “common centroid” placement is an example of a linear gradient compensation layout, but it occupies a large area on a chip and it is difficult to connect the elements with each other due to the significant distance between them and possible connection crossings [17]. The “regular” layout without gradient compensation was chosen as the smallest placement area with the simplest connection of elements. Script examples with these placements are shown in Fig. 4. Numbers from 0 to 16 in the matrix denote R-2R

```

a) Rmatrix =
[16 4 6 8 10 12 16 ;
14 5 7 9 11 13 14 ;
15 4 6 8 10 12 -1 ;
-1 2 3 2 1 0 -1 ;
-1 -1 -1 -1 -1 -1 -1 ;
-1 0 1 2 3 2 -1 ;
-1 12 10 8 6 4 15 ;
14 13 11 9 7 5 14 ;
16 12 10 8 6 4 16 ;] ;

b) Rmatrix =
[0 1 3 5 7 9 11 13 15 ;
-1 2 4 6 8 10 12 14 16 ;
-1 2 4 6 8 10 12 14 16 ;] ;
    
```

Fig. 4. Code example of the weighting elements matrix:  
*a* – “common centroid” placement; *b* – “regular” placement

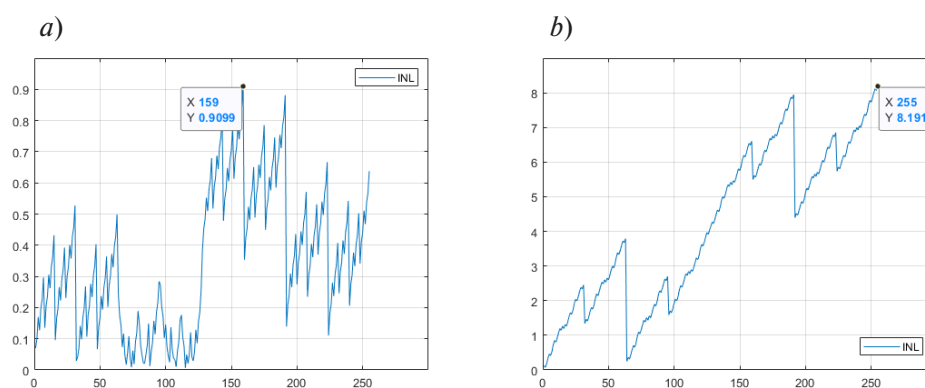


Fig. 5. INL plots for the central quadratic gradient simulation:  
*a* – “common centroid” placement; *b* – “regular” placement

matrix elements according to the numeration in Fig. 3, which includes the resistance of the given weighting element. The number “–1” denotes an empty cell.

Three types of gradients were simulated separately: linear, quadratic and central quadratic. The maximum gradient value was limited to 20 %. Each gradient was set on both axes. Taking the gradients into account, DAC output characteristics were calculated for two placements (“common centroid” and “regular”), as well as DNL and INL, scaled to the value of the minimum step of the transfer characteristic, which is LSB (least significant bit). The results of the modeling are given in Table 1.

Table 1

### Simulation results

Gradient type	Maximum value of DNL, LSB		Maximum value of INL, LSB	
	“regular” layout	“common centroid” layout	“regular” layout	“common centroid” layout
Linear	–6.894	$\sim 10^{-14}$	13.590	$\sim 10^{-14}$
Quadratic	–3.027	–0.901	6.234	2.174
Central quadratic	0.742	–3.553	0.910	8.191

For the linear gradient, the best placement was of the “common centroid” type. According to the modeling result, it allows INL of the order of  $10^{-14}$  LSB, which is comparable to the accuracy of MATLAB calculations.

For the quadratic gradient, the “common centroid” placement is less suitable than for a linear gradient, as INL in this case reaches 2.174 LSB. This value is higher than acceptable (INL can be considered acceptable if not higher than  $\pm 1$  LSB, acceptable DNL does not exceed  $\pm 0.5$  LSB). However, compared to the “regular” placement, the “common centroid” placement result was better.

For the central quadratic gradient, the best placement was the “regular” one. It gives the maximum DNL = 0.742 LSB and INL = 0.910 LSB, while in the “common centroid” arrangement these values are –3.553 LSB and 8.191 LSB, respectively. INL plots for this gradient are shown in Fig. 5.

### Conclusion

This paper considered the non-linearities in the R-2R DAC static characteristics caused by systematic errors of the weighting elements (resistances). A MATLAB script was developed to simulate these errors

in the form of matrix gradients and to calculate the static DAC characteristics taking into account these gradients for different weighting elements placement. INL and DNL were estimated for three types of gradients (linear, quadratic, central quadratic) and for two types of placements (“regular” and “common centroid”). The result shows that the “common centroid” placement is better for both linear and quadratic gradients. On the other hand, the “regular” placement is better for the central quadratic gradient. In addition, the MATLAB script written in the process of the research can be further used to model gradient impact on various R-2R DAC weighting element placements and DAC static characteristics.

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