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RESEARCH ON PHASE-FREQUENCY DETECTOR ALGORITHMS FOR FAST LOCKING PLL FREQUENCY SYNTHESIZERS

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Abstract. Methods of accelerating transient processes in frequency synthesizers based on a pulse phase-locked loop (PLL) using a coarse accelerating control before the PLL reaches small frequency errors with subsequent accurate phase control are briefly considered. To determine the need to turn on the coarse accelerating control, phase-frequency detectors (PFD) with saturation states are used. The article discusses four well-known algorithms of the PFD, which differ from each other in the conditions and direction of exit from the saturation states. It is shown that without changing the specifications of the elements of the PLL in saturation states, none of the algorithms of the PFD has any significant advantage. When changing the specifications of the elements of the PLL, the algorithm of the PFD, which, upon exiting the saturation states, goes into phase control of the opposite action, immediately after exiting the saturation states has more effective error elimination and, therefore, a more optimal resulting transient process.

Keywords: frequency synthesizer, phase-locked loop, fast locking, phase-frequency detector, states algorithm

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ИССЛЕДОВАНИЕ АЛГОРИТМОВ ЧАСТОТНО-ФАЗОВЫХ ДЕТЕКТОРОВ ДЛЯ БЫСТРОДЕЙСТВУЮЩИХ СИНТЕЗАТОРОВ ФАЗОВОЙ АВТОПОДСТРОЙКИ ЧАСТОТЫ

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Аннотация. Кратко рассмотрены методы ускорения переходных процессов в синтезаторах сетки частот на базе контура импульсной фазовой автоподстройки частоты (ФАПЧ) с использованием грубого ускоряющего воздействия до входа контура ФАПЧ в область малых рассогласований по частоте с последующей точной регулировкой по фазе. Для определения необходимости включения ускоряющего воздействия применяются частотно-фазовые детекторы (ИЧФД), имеющие состояния насыщения. Описаны четыре известных алгоритма работы ИЧФД, отличающиеся между собой условиями и направлением выхода из состояний насыщения. Показано, что без изменения параметров элементов контура ФАПЧ в состояниях насыщения ни один из алгоритмов не имеет существенного преимущества. При изменении параметров элементов контура ФАПЧ алгоритм ИЧФД, осуществляющий при выходе из состояний насыщения переход в фазовое управление противоположного воздействия, сразу после выхода из состояний насыщения имеет более эффективную отработку фазового рассогласования и, как следствие, наиболее оптимальный результирующий переходный процесс.

Ключевые слова: синтезатор сетки частот, фазовая автоподстройка частоты, ускорение переходного процесса, частотно-фазовый детектор, алгоритм перехода состояний

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Introduction

Frequency synthesizers based on a pulse phase-locked loop (PLL) are widely used in modern integrated circuits of communications and computing technology. Some of the main performances of PLL synthesizers are the output frequencies range, frequency and spectral resolution, the speed of transient processes (TP) of frequency setting. Further development of the functionality of the end products requires an increase in the performances of PLL synthesizers, including an increase in the speed of TP. One of the methods to increase the speed of TP is to use the mode of coarse accelerating control of the PLL until small frequency error is reached, followed by precise phase adjustment. Therefore, researches of the implementation of coarse accelerating control of the PLL are relevant.

The article gives a brief overview of methods for accelerating TP and researches the effectiveness of phase-frequency detector algorithms to accelerate the initial stage of TP in the coarse accelerating control mode and at the stage of transition to the state of phase error control.

Transient processes acceleration methods in PLL frequency synthesizers

Fig. 1 shows the block diagram of the integer-N PLL frequency synthesizer [1–3]. The PLL synthesizer uses a signal from an external source, e.g. a crystal oscillator, as a reference. The pulse phase-fre-

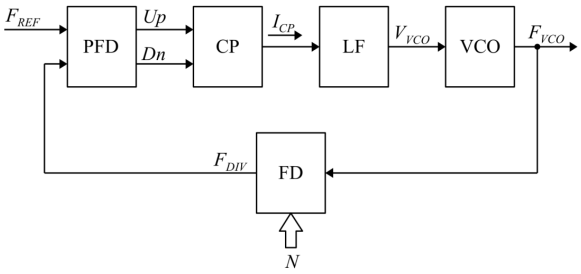

Fig. 1. Block diagram of the integer-N PLL frequency synthesizer

quency detector (PFD) generates signals Up or Dn, the duration of which is proportional to the time interval of alternately following signals of the reference frequency F_{REF} and the feedback frequency F_{DIV}. Based on these signals, the charge-pump (CP) generates width-modulated current pulses I_{CP} of the corresponding polarity, which produces voltage V_{VCO} at the impedance of the loop filter (LF). The frequency divider (FD) divides the output frequency F_{VCO} of the voltage controlled oscillator (VCO) by a factor N. The conversion of the phase error intervals of signals F_{REF} and F_{DIV} into a change in the control voltage V_{VCO} of the VCO carries out so that as a result, the PLL locks in and the output frequency FVCO is equal to the value of the reference frequency F_{REF} multiplied by a factor of N.

Damping of TP fluctuations and stability of the PLL are ensured by a phase margin at the bandwidth frequency. To ensure proper suppression of V_{VCO} voltage ripple caused by the output current pulses of the CP, the bandwidth frequency of the PLL should, as a rule, be at least 10 times lower than the frequency F_{REF}. At the same time, it should be borne in mind that above the bandwidth frequency of the PLL, the intrinsic phase noise of the VCO is transferred to the output frequency F_{VCO} without attenuation. Therefore, the value of the bandwidth frequency is a compromise between the duration of the TP and the magnitude of phase noise in the output frequency F_{VCO} [1–6].

The integer-N PLL was chosen to simplify the further narration, but the methods for accelerating TP considered below are also applicable to fractional-N PLL.

A direct solution to improve locking time in PLL is to increase the loop bandwidth, since the lock time is inverse bandwidth. However, it is also necessary to increase F_{REF}, which isn't always possible, since in the device with PLL, F_{REF} is often set or limited. For example, a higher F_{REF} value increases power consumption, which is limiting, especially in portable devices. Therefore, it is necessary to increase the speed capability of the PLL in the transient state while saving the required filtering capability in the steady state.

In the theory of automatic control, in order to ensure high performance in terms of both speed and accuracy of TP, combined control is widely used, when control actions are carried out in accordance with different criteria depending on the error value. Upon switching to a new output frequency or with a large error at the beginning of the TP, control should be carried out only in terms of ensuring the high adjustment speed. Then, when the error is decreased to a small value, the control changes to meet the fast damping of the TP fluctuations and ensure the filtering capability of the PLL. As a result of independent control at the initial stage and at the end of the TP, the contradiction between the speed and stability of the PLL decreases.

To decrease the duration of the initial stage of the TP, the methods of coarse accelerating control are used until the PLL reaches the small error. Among others, these methods include direct initial presetting of the output frequency of the VCO to approximately the required value and changing the specifications of the elements of the PLL [7].

Direct presetting of the output frequency of the VCO can be carried out by using either a VCO with the capability to switch output frequency subbands or presetting the control voltage of the VCO (for example, with a digital to analog converter) [7].

The preselection of the required subband of the output frequencies of the VCO can be carried out by changing the number of load capacitors or the output resistance in the signal generation circuits, by presetting the required operating current of the VCO, as well as by switching the number of delay cells in the ring of the VCO [2, 3, 7–9]. In this case, the process of initial presetting of the output frequency of the VCO can be considered practically inertia-free.

The initial presetting of the control voltage at the input of the VCO is carried out using the code corresponding to the required frequency [9–13]. In this case, the control voltage of the VCO varies depending on the production technological process variation of the elements of the VCO, the supply voltage and the temperature of the chip [6]. With the minimization of technological process standards, these problems increase, and as a result, eliminating the residual phase error due to an increase in the initial frequency error can bring the TP to the end much faster. In addition, the use of direct presetting of the control voltage of the VCO greatly complicates the circuit and increases the PLL area on the chip. Calibration of the control voltage codes of the presetting VCO for each chip leads to an even greater complication of the PLL frequency synthesizer and an increase in the cost of the end products [8].

An alternative to the methods of presetting the output frequency of the VCO is to change the structure and specifications of the elements of the PLL at the initial stage of TP until a small frequency error is reached [7, 14]. If the phase error of signals F_{REF} and F_{DIV} exceeds the value of $\pm 2\pi$ radians (but the value fewer than $\pm 2\pi$ radians can also be used [15–17]), the PLL switches to the coarse accelerating control. In this case, only the sign of the error of signals F_{REF} and F_{DIV} is taken into account, but its value isn't taken into account. As a result, the control is continuous and doesn't depend on the value of the phase error, which precludes the intrusion of beats in the control (phase slip cycles) and, thereby, accelerates the elimination of a large initial frequency error. When the output frequency F_{VCO} approaches the required value, the PLL returns to the phase control mode with a linear dependence on the phase error value.

To further reduce the initial stage of TP in the coarse accelerating control, loop bandwidth is increased by both a multiple increase in the amplitude of the output current of the CP and a change in the impedance of the LF [1–3, 5, 6, 15, 18–22]. The bandwidth can be increased with or without loop stability. After the PLL reaches a small phase error, the bandwidth is restored to its reference value.

Fig. 2 shows the block diagrams of the 2nd order LF with the capability of reducing the resistance R_Z in the coarse accelerating control at the initial stage of TP [1, 6, 22]. The LF has zero and pole frequencies and is an inertial proportional-integrating element in the PLL. The $R_Z C_Z$ performs frequency correction of the PLL to create the required phase margin and damping the fluctuations of TP. The LF has a maximum phase margin of up to –90° at the frequency that is the geometric mean of the zero and pole frequencies. When designing a PLL, the goal is for the open-loop unity gain frequency to be equal to this geometric mean frequency.

When the output current of the CP increases by a factor of K, the resistance R_Z is reduced by the square root of K to preserve the reference phase margin. This will also increase the bandwidth to the square root of K [2, 3, 19].

The resistances R_{Z1} and R_{Z2}, taking into account the residual resistance R_{SW1} of the closed switch SW_1, are calculated as

$$R_{Z2} = \frac{1}{2}\left(R_{ZL} - R_{ZF} + \sqrt{\left(R_{ZL} - R_{ZF}\right)\left(R_{ZL} - R_{ZF} + 4R_{SW1}\right)}\right),$$

$$R_{Z1} = R_{ZL} - R_{Z2},$$

where R_{ZL} is the required R_Z in phase control (switch SW_1 is open); R_{ZF} is the required R_Z in coarse accelerating control (switch SW_1 is closed).

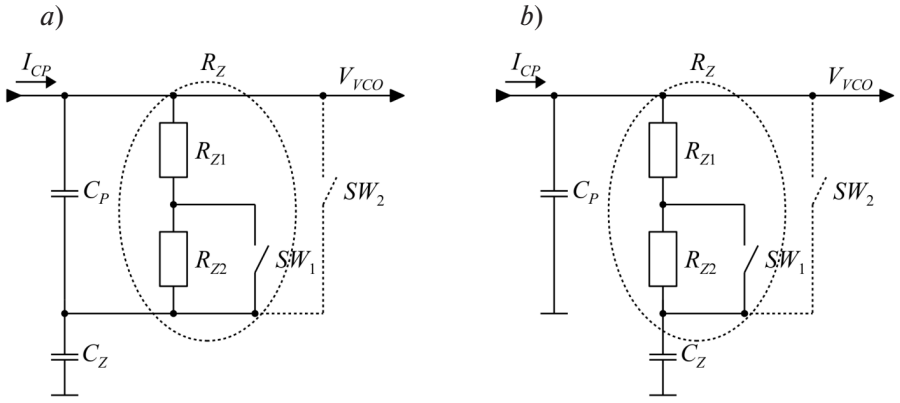

Fig. 2. Block diagrams of the 2nd order LF with the capability to reduce the resistance R_Z: *a* – series connection of C_P and C_Z; *b* – parallel connection of C_P and C_Z

The increasing overshoot of TP imposes limitations on increasing bandwidth in coarse accelerating control. However, to further accelerate the adjustment of the control voltage of the VCO, a further increase in the amplitude of the output current of the CP is required. To accelerate the recharge of the LF capacitors, in [5, 20] it is proposed to use an augmented set of amplitudes of the output current of the CP.

The method consists in shunting the resistor R_Z, synchronization of the counting start in the FD by the F_{REF} signal, and anticipatory exit of the PLL from the coarse accelerating control. This method allows increasing the output current of the CP and at the same time precluding large overshoot of TP.

The simultaneous increase in the output current of the CP and the shunting of R_Z cause the loss of stability of the PLL [6, 23]. In this case, at the moment when the PLL exits the coarse accelerating control, the voltage of the capacitor C_P at the LF of Fig. 2*a* is about zero, and at the LF of Fig. 2*b* it coincides with the voltage of the capacitor C_Z, which improves the initial conditions for damping the fluctuations of TP by the R_ZC_Z circuit when the PLL returns to phase error control.

Synchronization of the counting start in the FD by the F_{REF} signal contributes to the creation of favorable phase relations between the F_{REF} and F_{DIV} signals at the time of comparing their periods in the PFD [7, 14].

The anticipatory exit of the PLL from the coarse accelerating control is similar in effect to the differential component and is used to prevent large overshoot of TP due to the inertia of the PLL caused by the presence of a FD in the feedback. The anticipatory exit is realized by dividing the F_{VCO} frequency in the FD by a factor greater or less than the required N in the steady state, depending on what action (*Up* or *Dn*) the PLL is under.

Thereby, simultaneous and fast change in the control voltage V_{VCO} and a timely exit of the PLL from the coarse accelerating control is ensured when the output frequency of the VCO reaches a value close to the required one.

Also, other methods are used to accelerate the tuning of the control voltage V_{VCO} at the initial stage of TP. For example, the use of an additional CP connected directly to the capacitor C_Z, and the ratio of the current of the additional CP to the main one equals the ratio of the capacitances C_Z to C_P [2, 24]. In [25], the connection of a voltage repeater to be switched off in parallel to the resistor R_Z is considered. The repeater input is connected to the V_{VCO} circuit and, thereby, in the coarse accelerating control, the entire current of the CP is spent on recharging the capacitor C_P.

The block diagrams of the 2nd order LF with additional switches SW_2 shown in Fig. 2 are functionally equivalent to the diagrams shown in [26], where the PLL additionally contains units for detecting the synchronism in frequency and in phase. The control algorithm for switches SW_1 and SW_2 is as follows. At the beginning of TP, the FD and the PFD are reset to the initial state, the switches SW_1 and SW_2

are closed and the output current of the CP is increased. As a result, a high speed of V_{VCO} voltage adjustment is achieved. After detecting that the frequencies F_{REF} and F_{DIV} are close, the switch SW_2 is opened, the PFD and the PFD are reset to the initial state again, while the increased value of the output current of the CP remains. At the same time, the damping effect emerges and the PLL tries to eliminate the phase error. After detecting that the phases F_{REF} and F_{DIV} are close, the switch SW_1 is opened, the PFD and FD are reset again to the initial state, and the output current of the CP is returned to the reference value.

The requirements to further reduce the initial stage of TP lead to the combined use of a VCO preset and bandwidth increase, as, for example, in [27].

Research of algorithms for pulse phase-frequency detectors with saturation states

It is known that the dynamics of TP of frequency adjustment in the PLL when using coarse accelerating control largely depends on the algorithm for generating output control signals of the PFD. The simplest PFD has three states: two phase control states and a neutral retention state [1–3]. To implement coarse accelerating control, PFD with five or more algorithm states are used.

Fig. 3 shows the algorithms for PFD presented in [28–31]. The state designated as *Off* refers to the retention of charge on the capacitors of the LF. The LF capacitors are recharged in the groups of *Up* and *Dn* states. In phase control and with the alternating sequence of the F_{REF} and F_{DIV} signals, the PFD switches between the *Up* (*B*) or *Dn* (*E*) states and the *Off* state (*A*). The condition for changing the state of the phase control is the change in the sign of the phase error of the F_{REF} and F_{DIV} signals. Coarse accelerating control in the PLL is carried out when the PFD is in saturation states, designated as *Fast*.

For all the algorithms shown, switching to the saturation states is carried out after the arrival of the second F_{REF} or F_{DIV} pulse in a row, i.e., when the phase error of the F_{REF} and F_{DIV} signals increases by more than $\pm 2\pi$ radians. The conditions and direction of exit from the saturation states are different for the shown algorithms. Since the algorithms are symmetrical about the *Off* state, only the exit from the saturation state of the *Up* action is considered in detail.

For all algorithms, when the first F_{REF} pulse arrives, switching to the state of the phase control of the *Up* action is carried out. After the second consecutive impulse F_{REF}, switching to the *Fast* state is carried out. Outside of this, the algorithms differ from each other.

For the algorithm in Fig. 3*a*, when a single pulse F_{DIV} arrives, the *Up* state remains, but the PFD leaves the *Fast* state. Only two consecutive F_{DIV} pulses in the interval between two F_{REF} return the PFD to the *Off* state. With a large error between the F_{REF} and F_{DIV} frequencies, this algorithm precludes beats in the control (phase slip cycles), but periodically disables the coarse accelerating control.

For the algorithms of Fig. 3*b*, *c*, *d*, it is typical that one incoming F_{DIV} pulse doesn't bring the PFD out of the *Fast* state. For the algorithm in Fig. 3*b*, the second consecutive F_{DIV} pulse in the interval between F_{REF} pulses switches the PFD to the state of phase control, with the opposite action *Dn*. For the algorithm in Fig. 3*c*, the second consecutive F_{DIV} pulse between F_{REF} pulses returns the PFD to the *Off* state. For the algorithm in Fig. 3*d*, the second consecutive F_{DIV} pulse between F_{REF} pulses switches the PFD to the state of phase control, with the opposite action *Dn*, and the alternate arrival of the F_{REF} and F_{DIV} pulses returns the PFD to the *Off* state.

In terms of the theory of automatic control, the considered PLL is a pulse stabilization system, in which regulation is carried out by signals with pulse-width modulation. In addition, the considered PLLs have elements with variable parameters (CP + LF) and nonlinear correction (PFD) with complex algorithms for conditions and directions of exit from saturation states. These circumstances make the analytical study of the characteristics of the TP very difficult. Thus, mathematical modeling is widely used to study the TP characteristics in the practice of designing such PLLs. In this paper, the simulation was carried out in the Simulink environment [2, 32, 33].

To study the efficiency of the considered algorithms of the PFD for accelerating the initial stage of TP, the simulation of setting the output frequency F_{VCO} from a zero initial value for three control conditions when the PFD was in the *Fast* states was carried out:

• without using acceleration, i.e. without changing the specifications of the PLL elements;

• with acceleration by increasing the bandwidth by 2 times, i.e. increasing the output current of the CP by 4 times and reducing the resistance R_Z by 2 times;

• with acceleration by increasing the output current of the CP by 10 times, reducing the R_Z, using the synchronization of the FD by the pulses F_{REF} and anticipatory exit from coarse accelerating control.

In the simulation, the PLL was used with the following characteristics: input frequency 1 MHz, output frequency 100 MHz, bandwidth 100 kHz, phase margin 60°.

Results of frequency setting TP simulation

TP simulation diagrams of setting the output frequency to 100 MHz from the initial value of zero are shown in Fig. 4–6. From the diagrams, it is possible to draw conclusions about the control at different stages of TP, quantify the overshoot and duration. Common to all diagrams is that on the second cycle of the F_{REF} signal, i.e., when the phase error exceeds +2π radians, the PLL switches to the coarse accelerating control, which is designated by the *Fast* signal.

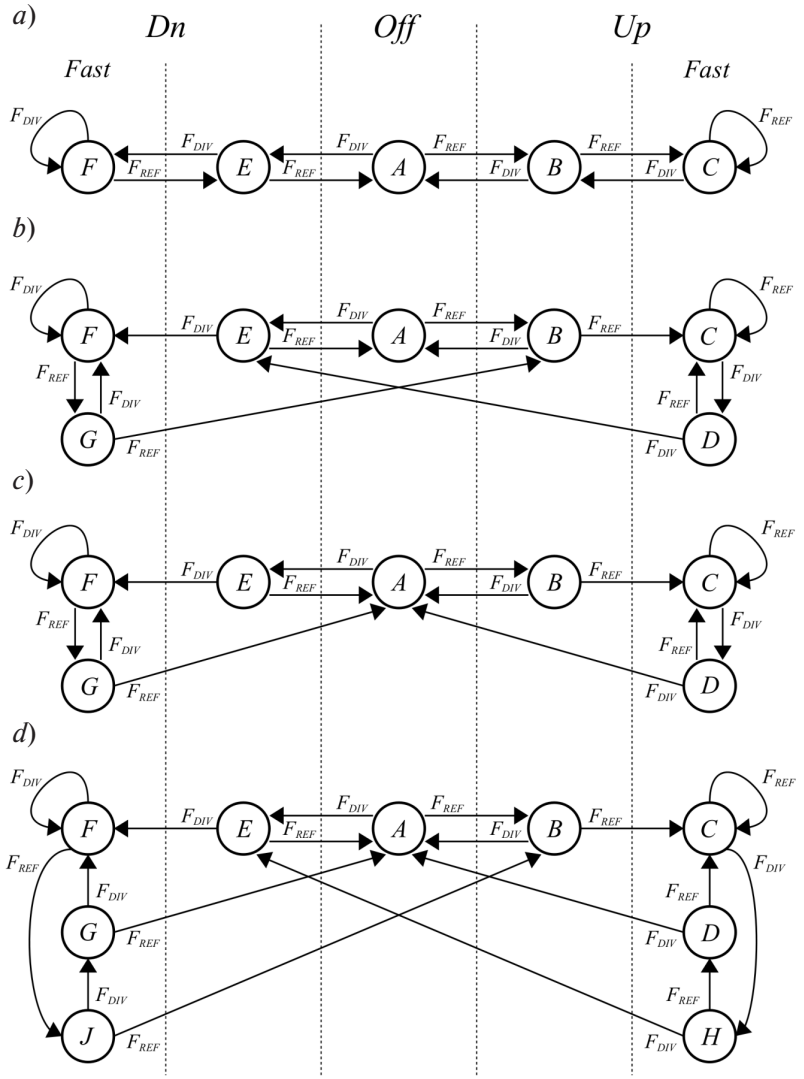

Fig. 3. Algorithms of PFD: *a* – [28, 29]; *b* – the first embodiment in [30]; *c* – the second embodiment in [30]; *d* – [31]

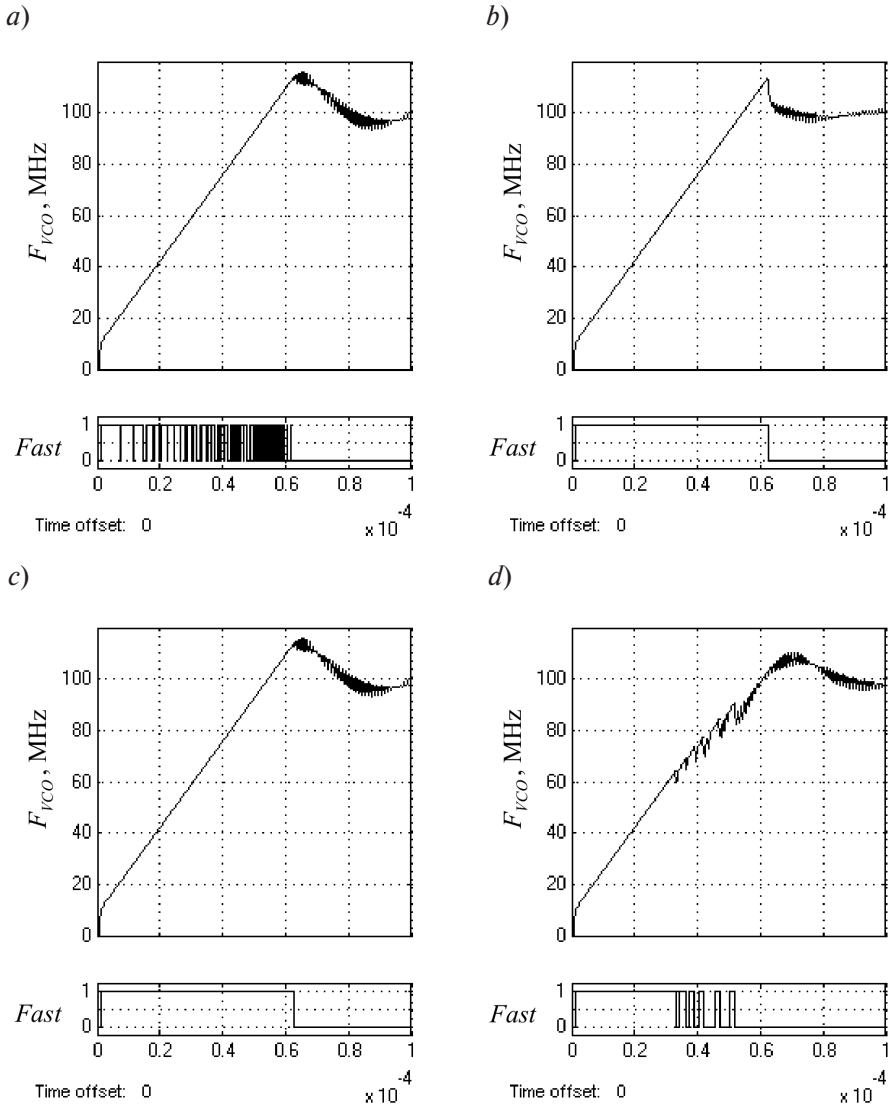

Fig. 4. TP diagrams of setting the frequency F_{VCO} without changing the specifications of the PLL elements in *Fast* mode when using the PFD of works: *a* – [28, 29]; *b* – the first embodiment in [30]; *c* – the second embodiment in [30]; *d* – [31]

Fig. 4 shows the TP diagrams of setting the output frequency F_{VCO} without changing the specifications of the PLL elements when the PFD was in the states *Fast*. All TP diagrams have overshoot. Refer to Fig. 4*a*. After switching the PFD to the *Fast* state, the pulses F_{DIV} that begin to arrive periodically switch the PFD to phase control, but this doesn't affect the slew rate of the output frequency F_{VCO} since the PFD remains in the *Up* state. In Fig. 4*b*,*c*, until a small frequency error is reached, the *Fast* state isn't reset and, therefore, the slew rate of the output frequency F_{VCO} coincides with that in Fig. 4*a*. For the diagram in Fig. 4*d*, even before the small error in frequency F_{VCO} is reached, the PFD periodically switches to the *Off* state, which slows down the initial stage of TP. This circumstance is due to the peculiarity of the algorithm used in Fig. 3*d*, which consists in the fact that with alternate arrival of pulses F_{REF} and F_{DIV}, the PFD performs premature exits from the *Fast* state to the *Off* state even before reaching a small frequency error.

After the final exit from the *Fast* state, the PFD switches between the states of phase control. For Fig. 4*a*,*c*, the diagrams of the stages of the end of TP coincide. For the diagram in Fig. 4*b*, after exiting the *Fast* state, the beginning of the process of setting the frequency F_{VCO} is the most optimal in comparison with other diagrams. This is due to the fact that when leaving the *Fast* state, the PFD switches to the opposite action *Dn* of phase control.

Fig. 5 shows TP diagrams with bandwidth doubled when the PFD is in the *Fast* states. In this case, the slew rate of the control voltage V_{VCO}, and, consequently, the slew rate of the value of the output frequency F_{VCO}, are quadrupled in comparison with Fig. 4.

For the diagram in Fig. 5*a*, even before the small error in frequency F_{VCO} is reached, single pulses F_{DIV} remove the PFD from the state *Fast*, while remaining in the *Up* state. The premature exit from the *Fast* state decreases the resulting slew rate of the F_{VCO} frequency. It is clear that until the vicinity of the required frequency is reached, the coarse accelerating control must operate continuously. For the dia-

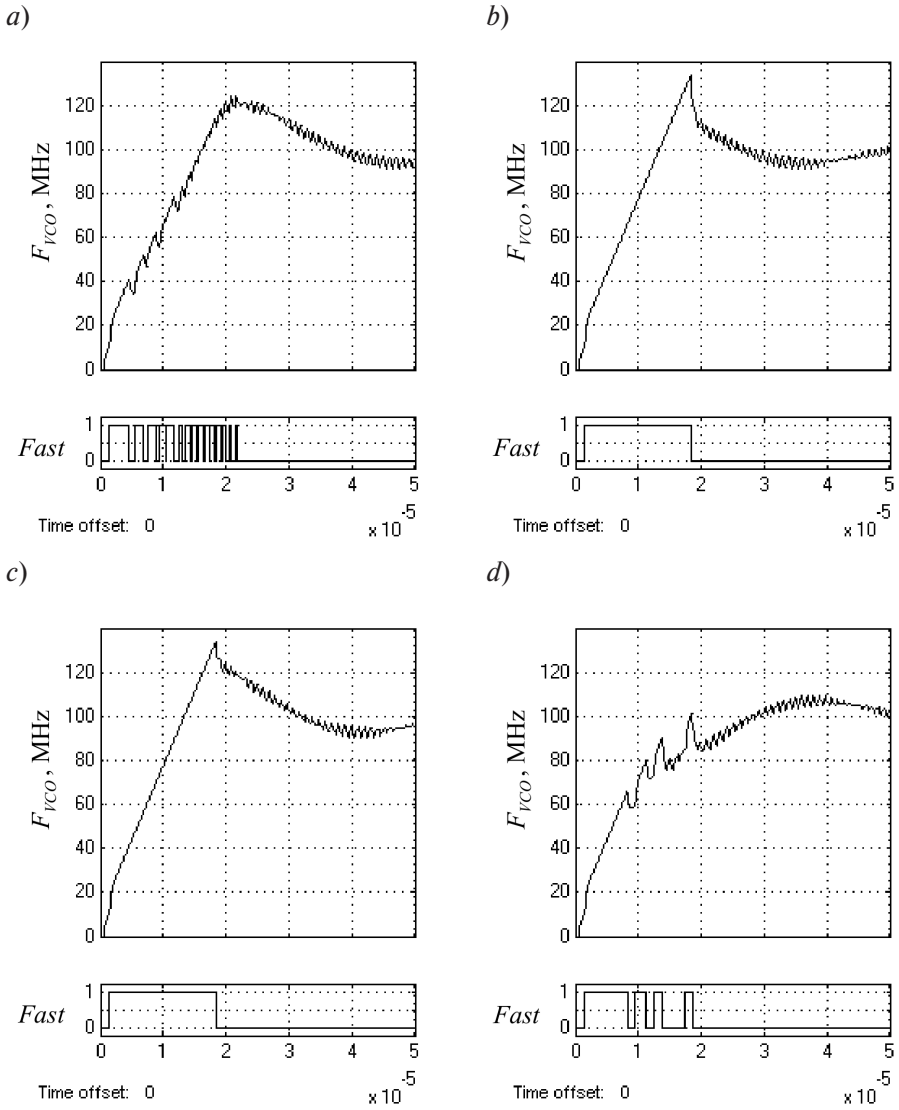

Fig. 5. TP diagrams of setting the frequency F_{VCO} with bandwidth doubled in *Fast* mode when using the PFD of works: *a* – [28, 29]; *b* – the first embodiment in [30]; *c* – the second embodiment in [30]; *d* – [31]

grams of Fig. 5*a*,*b*,*c*, the increased overshoot, in comparison with the diagrams of Fig. 4, is due to the fact that the bandwidth is increased, but anticipatory exit from the *Fast* mode isn't used. Small overshoot of the diagram in Fig. 5*d* is due to the periodic premature exit of the PFD from the *Fast* state. However, in this case, the rate of rise of the frequency V_{VCO} decreases.

Fig. 6 shows the diagrams of TP, where in the *Fast* state, an increase in the output current of the CP by 10 times, reduction of the R_Z, synchronization of the start of counting in the FD by pulses F_{REF} and anticipatory exit from coarse accelerating control are used. The *Synh* signal shows the moments of synchronization of the start of counting in the FD.

In the *Fast* state, the slew rate of the control voltage V_{VCO}, and therefore the value of the output frequency F_{VCO}, increase 10 times compared to Fig. 4 and 2.5 times compared to Fig. 5.

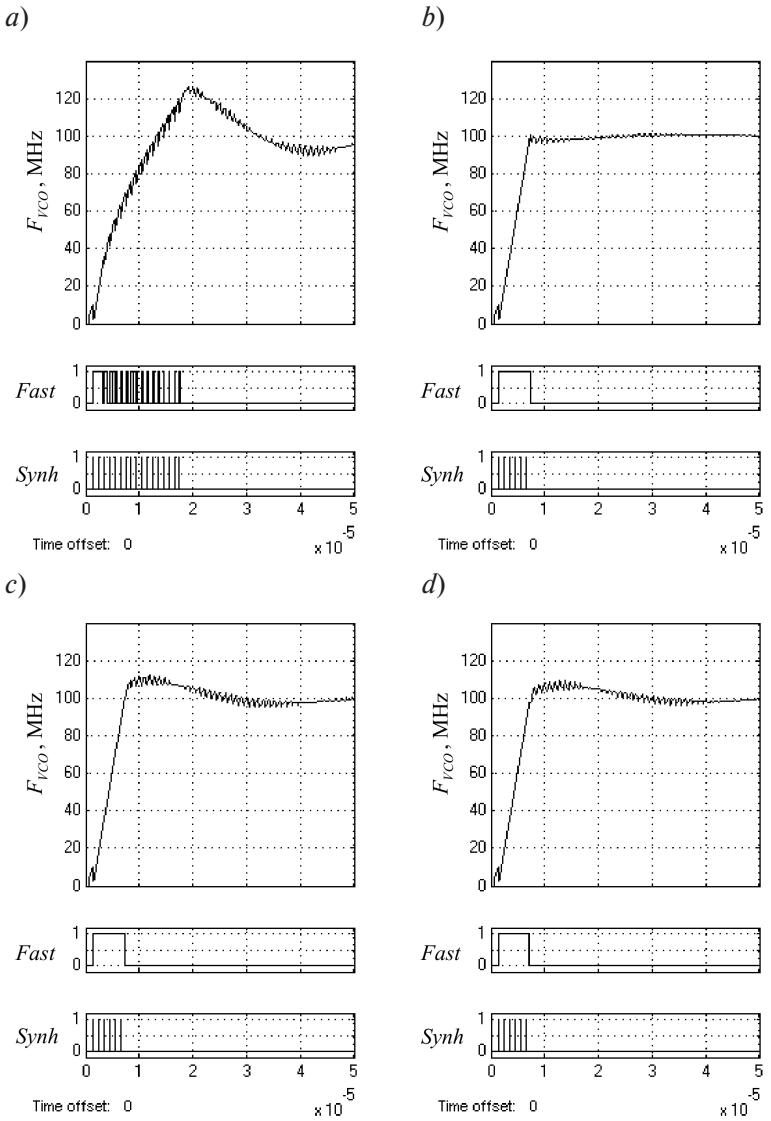

Fig. 6. TP diagrams of setting the frequency F_{VCO}, where in the *Fast* state a 10 times increase in the CP output current, reduction of the R_Z, synchronization of the FD and anticipatory exit from the *Fast* states are used with PFD of works: *a* – [28, 29]; *b* – the first embodiment in [30]; *c* – the second embodiment in [30]; *d* – [31]

For the diagrams of Fig. 6*a* as well as for the diagrams of Fig. 4*a* and Fig. 5*a*, the periodic premature exits of the PFD from the *Fast* state slow down the initial stage of the TP. The diagrams of Fig. 6*b*,*c*,*d* remain in the *Fast* state until the PLL reaches a small error.

The TP characteristics of Fig. 4–6 are summarized in Table 1. The duration of TP is given in the number of F_{REF} clocks.

Table 1

The TP characteristics of Fig. 4–6

Figure	TP overshoot, %	TP duration of F_{VCO} setting (in F_{REF} clocks) with an accuracy		
		5 %	1 %	0.1 %
4*a*	15.9	92	120	172
4*b*	13.5	63	104	153
4*c*	15.9	92	120	172
4*d*	10.4	79	123	172
5*a*	24.4	53	97	144
5*b*	33.6	42	86	135
5*c*	33.6	49	94	141
5*d*	9.5	44	89	140
6*a*	26.4	51	95	144
6*b*	1.32	7	37	87
6*c*	12.0	21	65	117
6*d*	9.2	19	64	114

Since the algorithms don't differ from each other when they are in phase control (switching between states A, B, E), then the durations of the TP of setting the frequency F_{VCO} from an accuracy of 1 to 0.1 % are practically identical and on average are 50 clocks. For the diagrams of Fig. 5 and 6, the duration of TP from an accuracy of 5 to 1 % takes on average 44 clocks, except for Fig. 6*b*. This difference is due to the fact that the overshoot of the TP in Fig. 6*b* is initially less than 5 % and the entry into this error range begins when the PFD is still in the *Fast* state. As a result, the diagram in Fig. 6*b* shows a close to optimal resulting TP, the minimum overshoot, and therefore, the total duration of the TP.

Based on the simulation results, the following conclusions can be drawn:

1. Without the use of an accelerating action at the initial stage of TP, none of the algorithms has a significant advantage. However, the algorithm in Fig. 3*b* looks preferable due to more efficient elimination of the error immediately after exiting the *Fast* states.

2. In case of accelerating by means of doubling the bandwidth, the TP using the algorithm in Fig. 3*b* also has an advantage, despite significant overshoot (more than 30 %).

3. The third considered method of accelerating the initial stage of TP is carried out by increasing the output current of the CP by 10 times, reduction of the *Rz*, synchronizing the start of counting in the FD by pulses F_{REF} and anticipatory exit from coarse accelerating control. In this case, the behavior of the TP using the algorithm in Fig. 3*b* already shows a significant advantage.

Conclusion

A common way to reduce the duration of TP in a PLL is to use an accelerating action until the PLL reaches a small error and, at the same time, to minimize overshoot. To determine the moment when the

accelerating action is turned on and to eliminate the phase slip cycles, PFD are used, which have saturation states when the phase error of the reference frequency and the feedback frequency exceeds $\pm 2\pi$ radians.

The algorithms of PFD presented in [28–31] are considered. To compare the efficiency of the algorithms of PFD, TP were simulated for conditions without acceleration and using two acceleration methods in saturation states of PFD (that is, in Fast states).

It is shown that without changing the specifications of the elements of the PLL in saturation states, none of the algorithms has any significant advantage. When changing the specifications of the elements of the PLL, the algorithm, which, upon exiting the saturation states, goes into phase control of the opposite action, immediately after exiting the saturation states has more effective error elimination and, therefore, a more optimal resulting TP.

Since the algorithms differ only in the conditions and direction of exit from the saturation state, these differences will appear only at the stage when the PLL eliminates large errors. After that, the duration of the TP depends on the initial overshoot and the required accuracy of setting the output frequency. Therefore, the more precise the setting of the output frequency is required, the less is the relative difference in the duration of TP for the considered algorithms and acceleration methods when the PFD is in a state of saturation.

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