Computing, Telecommunication and Control, 2022, Vol. 15, No. 2, Pp. 25–31.
Информатика, телекоммуникации и управление. 2022. Том 15, № 2. С. 25–31.

Research article
DOI: https://doi.org/10.18721/JCSTCS.15202
UDC 621.3.087.92

MODERN APPROACHES TO DESIGN OF MULTI-CHANNEL DELTA-SIGMA ADCS

V.I. Satyshev[1] ✉

[1] Peter the Great St. Petersburg Polytechnic University, St. Petersburg, Russian Federation

✉ sateshev5@yandex.ru

Abstract. Incremental delta-sigma ADC (IADC) and memoryless delta-sigma ADC are described. These two approaches allow to utilize a delta-sigma ADC, known for its increased resolution, in multi-channel systems due to the inter-sample interference suppression that two mentioned structures provide. In this paper, MATLAB/Simulink models of the mentioned structures are presented. In particular, limiting blocks are added to take into account nonlinearities due to finite power supply of integrators; coefficients of delta-sigma modulators were selected so as to maximize their signal-to-noise ratio; parameters of the raised cosine filter were selected to minimize crosstalk between channels. Results of simulations, namely power spectral density of the output signals and signal-to-noise ratio of the output signals, confirm operability of the described structures.

Keywords: analog-to-digital converter, delta-sigma modulation, inter-sample interference, incremental delta-sigma ADC, memoryless delta-sigma ADC

Citation: Satyshev V.I. Modern approaches to design of multi-channel delta-sigma ADCs. Computing, Telecommunications and Control, 2022, Vol. 15, No. 2, Pp. 25–31. DOI: 10.18721/JCSTCS.15202

Научная статья
DOI: https://doi.org/10.18721/JCSTCS.15202
УДК 621.3.087.92

СОВРЕМЕННЫЕ ПОДХОДЫ К ПРОЕКТИРОВАНИЮ МНОГОКАНАЛЬНЫХ ДЕЛЬТА-СИГМА АЦП

В.И. Сатышев[1] ✉

[1] Санкт-Петербургский политехнический университет Петра Великого, Санкт-Петербург, Российская Федерация

✉ sateshev5@yandex.ru

Аннотация. Рассмотрены инкрементальные дельта-сигма АЦП (IADC) и дельта-сигма АЦП без эффекта памяти. Данные подходы позволяют использовать дельта-сигма АЦП, известные высоким разрешением, в многоканальных системах, благодаря подавлению межвыборочной интерференции (ISI), которая достигается в двух рассматриваемых структурах. Приведены модели указанных структур в MATLAB/Simulink. В частности, введены ограничивающие блоки для учета нелинейных свойств реальных интеграторов, обусловленных конечностью напряжения питания; коэффициенты дельта-сигма модуляторов выбирались таким образом, чтобы максимизировать их отношение сигнал/шум; выбор параметров фильтра приподнятого косинуса проводился с целью минимизации межвыборочной интерференции в каналах. Результаты моделирований (спектральная плотность мощности выходных сигналов, отношение сигнал/шум выходных сигналов) подтверждают работоспособность рассматриваемых структур.

Ключевые слова: аналого-цифровой преобразователь, дельта-сигма модуляция, межвыборочная интерференция, инкрементальный дельта-сигма АЦП, дельта-сигма АЦП без эффекта памяти

Для цитирования: Satyshev V.I. Modern approaches to design of multi-channel delta-sigma ADCs // Computing, Telecommunications and Control. 2022. Т. 15, № 2. С. 25–31. DOI: 10.18721/JCSTCS.15202

Introduction

Electronic signals can be divided into two distinct categories: analog signals, which are continuous in time and amplitude, and digital signals, which could be presented as a set of discrete values. Digital systems and devices for storing and processing information have become widespread in recent decades. However, all of the signals that can be collected via physical processes, such as human speech or temperature measurements, are analog. That rises a problem of converting such signals into digital form so that they could be processed in digital systems. The devices that carry out such a conversion are known as analog-to-digital converters or ADCs.

In practice the necessity of using one ADC to digitize several analog channels might arise. That process is known as multiplexing an ADC. There are many types of ADCs, and among them delta-sigma ADCs are known to achieve the highest resolution thanks to oversampling and the noise shaping effect [1, 2]. Unfortunately, it is not possible to use conventional delta-sigma ADCs in multi-channel devices due to the inter-sample interference (ISI). The problem of ISI also known as crosstalk is demonstrated in Fig. 1.

The aim of this work is to present two modern approaches to design a delta-sigma ADC in a way that it could be used in a multi-channel system, that is it is free of inter-sample interference.

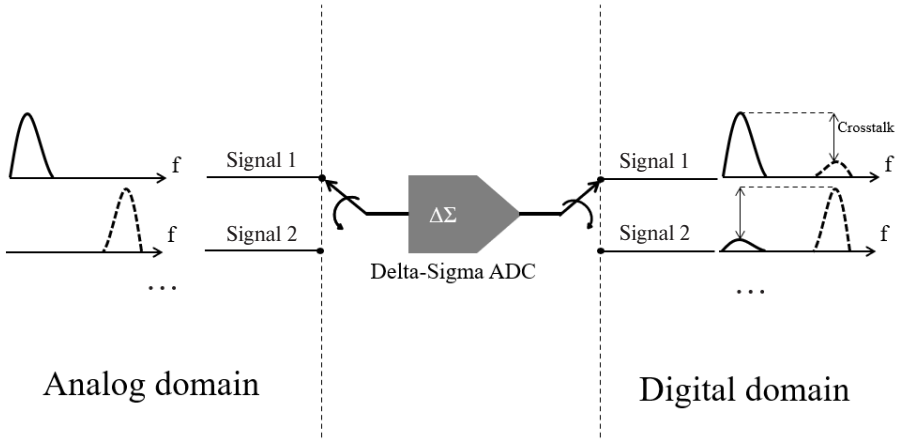

Fig. 1. Multiplexing a conventional delta-sigma ADC

Incremental delta-sigma ADCs

The first approach to design a multi-channel delta-sigma ADC is to use an incremental delta-sigma ADC (IADC). The main feature of IADC is the presence of a global reset pulse. The memories of both analog part and digital part of the ADC are reset at the beginning of the conversion of the subsequent analog signal sample. Thereby it is possible to completely remove ISI from the system. Moreover, since the delta-sigma modulators (DSMs) of such structures usually have finite impulse response, it is possible to use a finite impulse response decimation filter in contrast to much harder to implement infinite impulse response filters that are usually favored in conventional delta-sigma ADCs. The implementation of the decimation filter in this structure can be as straightforward as a cascade of integrators (CoIs). Other advantages of incremental structures include low latency and less tendency to idle tones.

The main disadvantage of incremental structures is increased thermal noise compared to conventional structures. To keep the same value of signal-to-noise ratio (SNR) as in conventional structures, it is necessary to increase the size of the input capacitor which results in higher power consumption of the amplifier that drives it [3–7]. There is a number of different approaches to improve characteristics

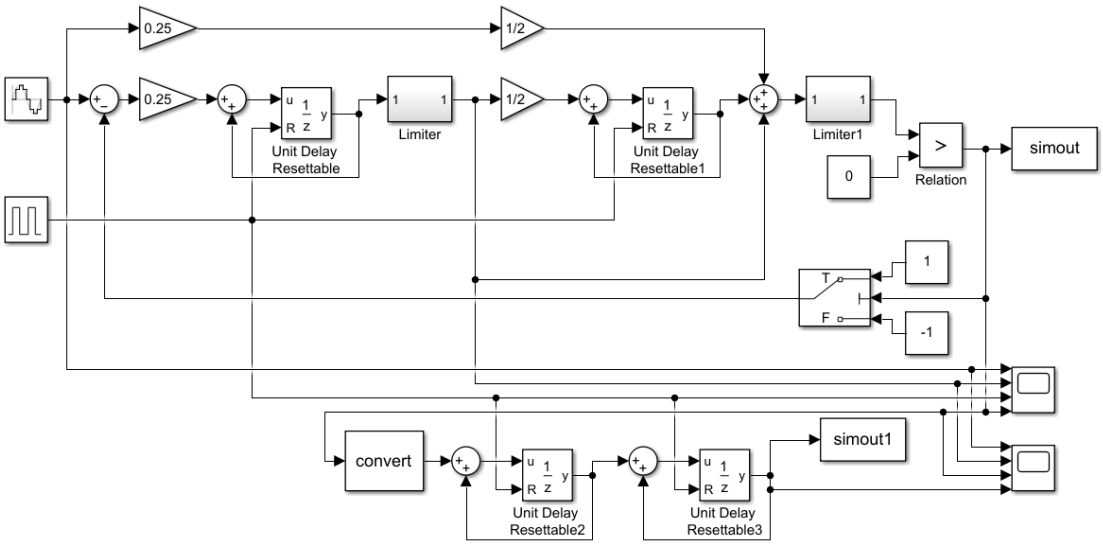

Fig. 2. Model of a second-order IADC in Simulink

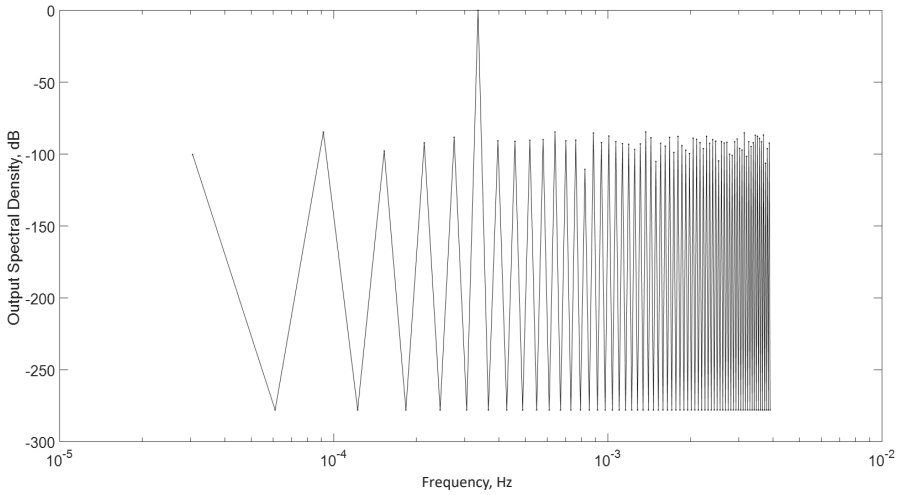

Fig. 3. Spectral density of the output signal after decimation

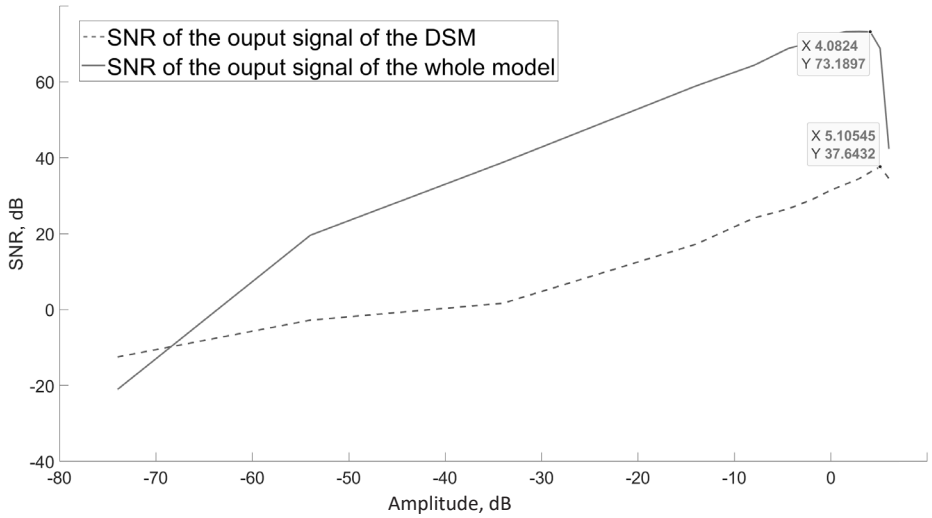

Fig. 4. Dependence of SNR from input amplitude

of incremental structures such as IADC with extended counting [8–11], hardware-sharing IADC [12], multi-step IADC [13–15], zoom ADC [16].

A second-order IADC was simulated in MATLAB/Simulink and is presented in Fig. 2. The model consists of a second-order delta-sigma ADC and two integrators that filter out the quantization noise. The decimation is carried out in a MATLAB script. In order to implement reset, functionally resettable unit delay blocks are used. Limiter blocks are added to take into account possible nonlinearities that could be created by real integrators due to limitations of power supply. Coefficients of delta-sigma modulator are selected so as to maximize SNR. Simulation results are presented in Fig. 3, 4.

Simulation results show that the reset pulses lead to a dramatic SNR decrease of the DSM output signal compared to conventional structures, but the SNR of the IADC as a whole remains good enough. As stated before, it is possible to add a multiplexer to the input of this model and configure the reset pulses in a way that would erase the memories of DSM and filter integrators at the beginning of each subsequent analog signal so as to achieve a zero ISI multi-channel conversion.

Memoryless delta-sigma ADCs

Another approach to design a multi-channel delta-sigma ADC is to use a memoryless delta-sigma ADC. This type of ADC relies heavily on implementing the decimation filter as a Nyquist filter, which is commonly used in communication systems. By utilizing zeros in its impulse response, it is possible to achieve a great ISI suppression. The main advantage of this structure comparing to IADC is that it achieves higher SNR because the impulse response of its decimation filter is not limited by the reset pulses which leads to narrower transition width and higher stop-band attenuation of the frequency response. That results in better overall noise suppression [17]. The principle of operation of the memoryless-type system is as follows. Let f_s be the oversampled DSM clock frequency, M – the oversampling ratio. Then if an analog signal is sampled at the frequency of f_s/M, up-sampled by a factor of M, passed through the DSM and Nyquist filter, the resulting signal would have zero ISI once in every M samples. These samples can be extracted by down-sampling the resulting signal by a factor of M (Fig. 5) [18].

A memoryless delta-sigma ADC utilizing a third-order DSM and a 4-bit quantizer was simulated in MATLAB/Simulink and is presented in Fig. 6. The model consists of a switch that acts as multiplexer, an upsample block, a third-order DSM, a 4-bit ADC-DAC structure (quantizer), a raised cosine decimation filter, which is a popular Nyquist filter, and two switches that act as a demultiplexer. Results of simulation are presented in Fig. 7.

Results of the simulations show that the memoryless delta-sigma ADC shown in Fig. 6 achieves a low noise level, which results in the SNR value of 81.9 dB, and great ISI suppression. The value of crosstalk between different channels is –94.5 dB.

Conclusion

Two modern approaches to design a multi-channel delta-sigma ADC are described. These structures are suitable for multi-channel systems as they aim to suppress the inter-sample interference, that limits

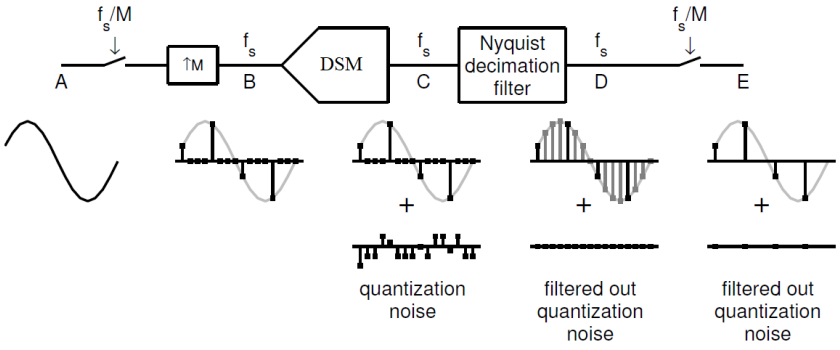

Fig. 5. Block diagram of memoryless delta-sigma ADC

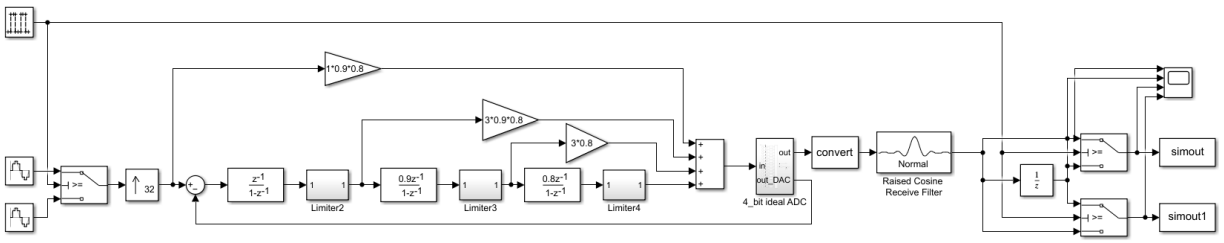

Fig. 6. Model of memoryless delta-sigma ADC in Simulink

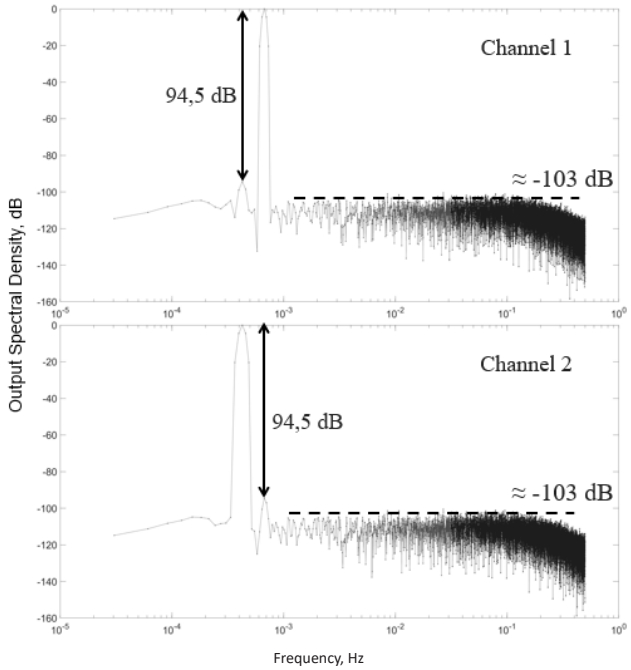

Fig. 7. Spectral density of the output signals

the usage of conventional delta-sigma ADCs in such systems. The MATLAB/Simulink simulation results of the second-order incremental delta-sigma ADC (IADC) and the third-order memoryless delta-sigma ADC are presented.

REFERENCES

1. **Kozlov A.S., Pilipko M.M.** A second-order sigma-delta modulator with a hybrid topology in 180nm CMOS. *2020 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering*, St. Petersburg and Moscow, Russia, 2020, Pp. 144–146. DOI: 10.1109/EIConRus49466.2020.9039246

2. **Korotkov A.S., Morozov D.V., Pilipko M.M., Yenuchenko M.S.** Sigma-delta ADC on SOI technology for working at high temperatures. *Radioelectronics and Communications Systems*, 2020, Vol. 63, no. 11, Pp. 586–595. DOI: 10.3103/S0735272720110035

3. **Tan Z., Chen C.H., Chae Y., Temes G.C.** Incremental delta-sigma ADCs: A tutorial review. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2020, Vol. 67, no. 12, Pp. 4161–4173. DOI: 10.1109/TCSI.2020.3033458

4. **Markus J., Silva J., Temes G.C.** Theory and applications of incremental delta-sigma converters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2004, Vol. 51, no. 4, Pp. 678–690. DOI: 10.1109/TCSI.2004.826202

5. **Kavusi S., Kakavand H., Gamal A.E.** On incremental sigma-delta modulation with optimal filtering. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2006, Vol. 53, no. 5, Pp. 1004–1015. DOI: 10.1109/TCSI.2006.870218

6. **Chen C.H., He T., Zhang Y., Temes G.C.** Incremental analog-to-digital converters for high-resolution energy-efficient sensor interfaces. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2015, Vol. 5, no. 4, Pp. 612–623. DOI: 10.1109/JETCAS.2015.2502135

7. **Chae Y., et al.** A 2.1 M Pixels, 120 Frame/s CMOS image sensor with column-parallel delta-sigma ADC architecture. *IEEE Journal of Solid-State Circuits*, 2011, Vol. 46, no. 1, Pp. 236–247. DOI: 10.1109/JSSC.2010.2085910

8. **Agah A., Vleugels K., Griffin P.B., Ronaghi M., Plummer J.D., Wooley B.A.** A high-resolution low-power incremental sigma-delta ADC with extended range for biosensor arrays. *IEEE Journal of Solid-State Circuits*, 2010, Vol. 45, no. 6, Pp. 1099–1110. DOI: 10.1109/JSSC.2010.2048493

9. **Harjani R., Lee T.A.** FRC: A method for extending the resolution of Nyquist rate converters using oversampling. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 1998, Vol. 45, no. 4, Pp. 482–494. DOI: 10.1109/82.663805

10. **Maeyer J. De, Rombouts P., Weyten L.** A double-sampling extended-counting ADC. *IEEE Journal of Solid-State Circuits*, 2004, Vol. 39, no. 3, Pp. 411–418. DOI: 10.1109/JSSC.2003.822903

11. **Lee C.C., Flynn M.P.** A 14 b 23 MS/s 48 mW resetting sigma-delta ADC. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2011, Vol. 58, no. 6, Pp. 1167–1177. DOI: 10.1109/TCSI.2010.2097716

12. **Kim J.H., et al.** A 14b extended counting ADC implemented in a 24Mpixel APS-C CMOS image sensor. *2012 IEEE International Solid-State Circuits Conference*, 2012, Pp. 390–392. DOI: 10.1109/ISSCC.2012.6177060

13. **Chen C.H., Zhang Y., He T., Chiang P.Y., Temes G.C.** A micro-power two-step incremental analog-to-digital converter. *IEEE Journal of Solid-State Circuits*, 2015, Vol. 50, no. 8, Pp. 1796–1808. DOI: 10.1109/JSSC.2015.2413842

14. **Zhang Y., Chen C.H., He T., Temes G.C.** Multi-step extended-counting analogue-to-digital converters. *Electronics Letters*, 2013, Vol. 49, no. 1, Pp. 30–31. DOI: 10.1049/el.2012.3655

15. **Zhang Y., Chen C.H., He T., Temes G.C.** A 16 b multi-step incremental analog-to-digital converter with single-opamp multi-slope extended counting. *IEEE Journal of Solid-State Circuits*, 2017, Vol. 52, no. 4, Pp. 1066–1076. DOI: 10.1109/JSSC.2016.2641466

16. **Chae Y., Souri K., K. Makinwa A.A.** A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV Offset. *IEEE Journal of Solid-State Circuits*, 2013, Vol. 48, no. 12, Pp. 3019–3027. DOI: 10.1109/JSSC.2013.2278737

17. **Kumar R.S.A., Behera D., Krishnapura N.** Reset-free memoryless delta–sigma analog-to-digital conversion. **IEEE Transactions on Circuits and Systems I: Regular Papers**, 2018, Vol. 65, no. 11, Pp. 3651–3661. DOI: 10.1109/TCSI.2018.2854707

18. **Behera D., Krishnapura N.** A 2-channel 1MHz BW, 80.5 dB DR ADC using a DS modulator and zero-ISI filter. *ESSCIRC 2014 – 40th European Solid State Circuits Conference* (*ESSCIRC*), 2014, Pp. 415–418. DOI: 10.1109/ESSCIRC.2014.6942110

INFORMATION ABOUT AUTHOR / СВЕДЕНИЯ ОБ АВТОРЕ

Vladislav I. Satyshev
Сатышев Владислав Игоревич
E-mail: sateshev5@yandex.ru

Submitted: 24.06.2022; Approved: 28.07.2022; Accepted: 25.08.2022.
Поступила: 24.06.2022; Одобрена: 28.07.2022; Принята: 25.08.2022.