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INFLUENCE OF ALGORITHM PARAMETERS ON STATIC NONLINEARITY IN SWITCHING-BASED CALIBRATIONS FOR DACS

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Abstract. This paper presents a comparative study of nonlinearity reduction by different algorithms of switching-based calibration method for DACs. Based on the known algorithms, one general parametric algorithm is proposed. The introduced parameters are a resolution of primary array and numbers of folding and decoupling operations. The intermediate options of such a general algorithm, defined by the parameters combination, are called “algorithm cases”. The algorithm cases are compared by the efficiency of static nonlinearity reduction in presence of random and systematic errors. For both errors, the folding operation improves DNL in contrast with the decoupling operation, which deteriorates it. The increment of folding operations number lowers the presence of systematic drift in DNL, which completely disappears at the maximum number. In the case of INL, the impact of both operations is determined by the elements order. If elements values depend on their indices, the folding operation deteriorates INL in contrast with the decoupling operation, which improves it. All fully unarized arrays provide the INL reduction, but do not decrease DNL.

Keywords: digital-to-analog converter, digital calibration, switching-based algorithm, mismatch, nonlinearity reduction, DNL, INL

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ВЛИЯНИЕ ПАРАМЕТРОВ АЛГОРИТМА НА СТАТИЧЕСКУЮ НЕЛИНЕЙНОСТЬ В КОММУТАЦИОННЫХ КАЛИБРОВКАХ ЦАП

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Аннотация. Проведено сравнительное исследование снижения нелинейности ЦАП различными алгоритмами коммутационного метода калибровки. На основе известных алгоритмов представлен общий параметрический алгоритм. Предложенными параметрами алгоритма являются разрядность исходного массива и количество операций объединения и рассоединения. Промежуточные случаи общего алгоритма, определяющиеся комбинацией параметров, называются «случаями алгоритма». Проведено сравнение случаев алгоритма между собой по эффективности снижения статической нелинейности в присутствии случайной и систематической ошибок. Для обоих типов ошибок операция объединения улучшает DNL в отличие от операции рассоединения, ухудшающей её. Увеличение количества операций объединения снижает влияние систематического ухода в зависимости DNL, полностью исчезающего при максимальном количестве операций. В случае INL влияние обеих операций зависит от того, в каком порядке находятся элементы. Если наблюдается зависимость значений элементов от их индексов, то операция объединения ухудшает INL в отличие от операции рассоединения, которая её улучшает. Все массивы элементов, имеющие унарную архитектуру, демонстрируют снижение INL, однако не уменьшают DNL.

Ключевые слова: цифро-аналоговый преобразователь, цифровая калибровка, коммутационный алгоритм, отклонение, снижение нелинейности, дифференциальная нелинейность, интегральная нелинейность

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Introduction

A digital-to-analog converter (DAC) is a significant interface device, which is implemented in modern electronic communication systems for converting an input digital code into a corresponding output analog signal, that can be represented as current or voltage. The conversion process is realized due to DAC's weighting elements (or shortly "elements") forming an analog signal proportionally to their values, or weights. In this paper, as for the elements, current sources are considered.

According to the ratio of elements weights, three common DACs architectures are highlighted: unary, binary and segmented. In a unary architecture, all elements are identical in their weights (also called "unary-weighted elements") and their ratio equals 1. In a binary architecture, elements are binary-weighted, which means that their weights have a ratio as power of 2. As for the segmented architecture, it is constructed from both unary and binary architecture parts called "segments". In Fig. 1, there are all three common architectures of DACs with a representation of elements in each architecture.

For a correct conversion result, such characteristics of DAC transfer curve as linearity and monotonicity are substantial and require the elements weights ratio to be precise regarding the nominal ratio.

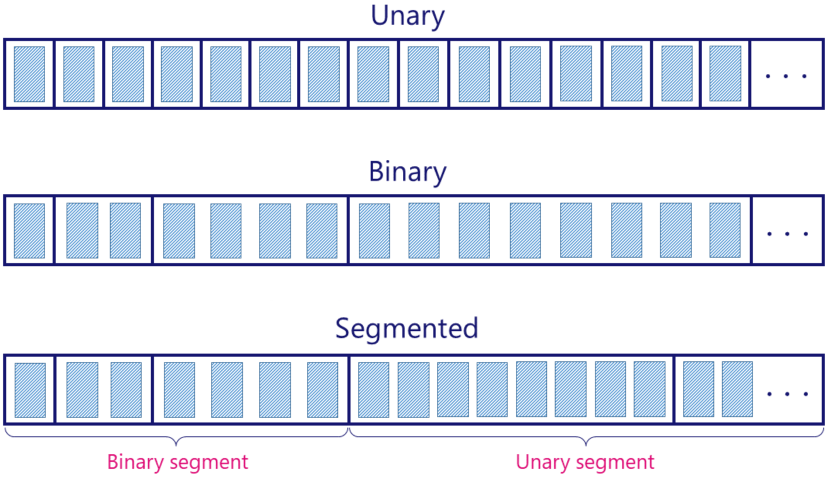

Fig. 1. Three common architectures of DACs

However, with the fabrication of integrated circuits, the elements mismatches unavoidably appear and deteriorate the accuracy of elements ratio, resulting in nonlinearity, or even nonmonotonicity, of transfer curve. Moreover, such unpleasant effects as aging, parasitic components and temperature deviations can also have an impact on further degradation of linearity. The mentioned issues are critical and make design of high-resolution (over 12 bits) DACs with a linear transfer curve quite challenging. In order to reduce the deteriorative impact of errors on DAC linearity and weaken the requirements for elements accuracy, a great number of electronic calibration methods was presented in [1–5] and classified in [6].

Among all calibration methods described in the classification, one particular method, i.e. switching-based calibration method, stands out due to minimization of the analog part. There is a great diversity of implementations of this calibration method (or just "algorithms"). These algorithms are also discussed thoroughly and classified in [7]. One of the introduced criteria for the classification is presence or absence of redundant elements, and the algorithms with the latter one are an object of this research. Some works did a comparison of such algorithms in terms of efficiency in nonlinearity reduction [8, 9], but provided poor coverage of intermediate implementations for the calibration method. Moreover, they do not study a static performance for the discussed algorithms in presence of systematic errors, as it was done for a dynamic performance in [8].

The goal of this research is to provide a comparative analysis of nonlinearity reduction by different implementations of switching-based calibration method in presence of both random and systematic errors. Additionally, this paper proposes a generalization of the known implementations providing intermediate options called "algorithm cases".

The present paper is organized as follows. In Section 1, the basic operations of switching-based calibration method are introduced. Then, a description of a general algorithm for switching-based calibration method is presented in Section 2. In Section 3, the simulation results for algorithm cases in presence of random and systematic errors are discussed. Based on the results, the comparison of considered algorithm cases by their efficiency in nonlinearity reduction is provided. Finally, in Section 4, the conclusions of the present work are drawn.

1. Basic operations

The principle of switching-based calibration method without redundant elements lies in changing the switching pattern for elements in an initial non-calibrated array. The initial array consists of 2^N unary-weighted elements (N is a DAC resolution) and further is called the primary array. The switching pattern is changed by means of elements indices reordering. The reordering procedure is based on two

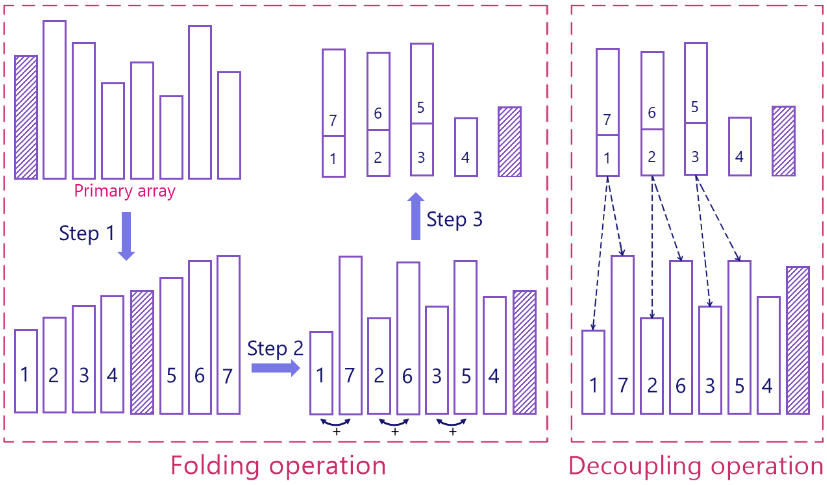

Fig. 2. The folding and decoupling operations

basic operations, folding and decoupling, which are applied to the primary array of elements as illustrated in Fig. 2. Here, rectangles heights correspond to the elements values.

To perform the folding operations, the 3 following steps must be done. At Step 1, the elements of primary array are compared with each one by their values and sorted in an ascending order. Then, the sorted elements change their places as it is shown in Step 2, so the couples of elements are created. Each couple contains the smallest elements preceding the greatest. At the final Step 3, the elements in couples are united. There is also a shaded dummy element in the array, which may be not involved in unification and can be absent. The result of folding operation is a segmented array with a decreased resolution of unary segment by one bit and with an increased resolution of binary segment by one bit.

The decoupling operation is performed with the application of only one step – the decomposition of previously united elements. It should be noted that after the decoupling all elements are placed in their order before unification. As the result, this operation increases the resolution of the unary array by one bit, which corresponds to the decrease in the resolution of the binary array. The number of decoupling operations cannot exceed the number of folding operations.

2. Description of general algorithm

Based on the previously known implementations [5, 9, 10], one general parametric algorithm is proposed. The algorithm depends on the following parameters: N is a primary array resolution, F and D are numbers of folding and decoupling operations respectively. A certain combination of N, F and D gives an individual algorithm case. In Fig. 3, a table of all algorithm cases is presented. The resolution of primary array N defines the maximum numbers of F and D. Colored areas in the table correspond to existent algorithm cases, while grayed out areas represent impossible cases of algorithm due to unrealizable combination of F and D.

It can be seen that with the increment of N the maximum numbers of folding and decoupling operations F and D also increase. Thus, the number of possible or existent algorithm cases grows with an arithmetic progression. The sum of arithmetic progression S_n is obtained by

$$S_n = \left(\frac{a_1 + a_n}{2}\right) \times n,$$

where a_1 and a_2 are the first and last numbers in numerical sequence, n is a number of elements in the sequence. The a_1 is the number of algorithm cases for a row with $F = 1$ in Fig. 3, a_2 is the number of

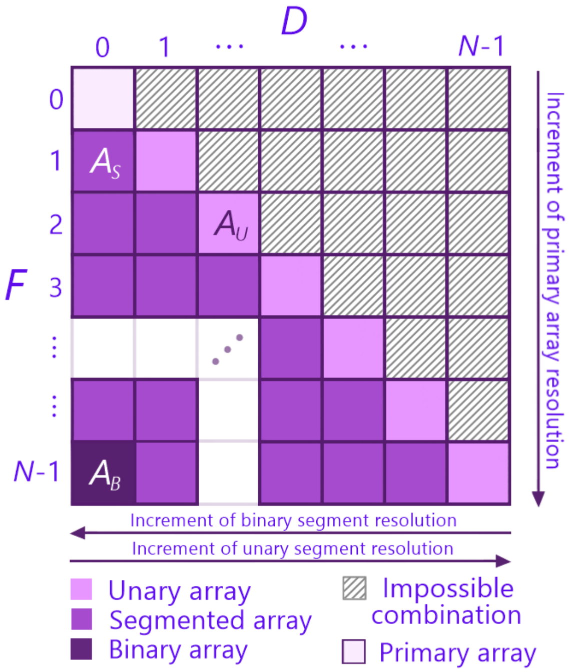
D
0
1
...
...
N-1
F
0
1
2
3
⋮
⋮
N-1
A_S
A_U
A_B
Increment of primary array resolution
Increment of binary segment resolution
Increment of unary segment resolution
Unary array
Segmented array
Binary array
Impossible combination
Primary array

Fig. 3. The table of algorithm cases and corresponding architectures

algorithm cases for a row with $F = N - 1$ and n is the number of rows. So, the final result for the number of existent algorithm cases is:

$$M_{ex} = \frac{(N-1)(N+2)}{2}.$$

According to the combinations of F and D, there are three types of algorithm cases which allow to obtain either binary, or unary or segmented architecture of calibrated array. As it was mentioned before, the folding and decoupling operations change the resolutions of unary and binary segments of calibrated array, thus the resolutions can be obtained by the following expressions, where N_U and N_B are resolutions of unary and binary segments respectively:

$$N_B = F - D,$$
$$N_U = N - N_B = N - F + D.$$

In order to construct the desired architecture of calibrated array, corresponding requirements for the numbers of folding and decoupling operations must be satisfied. So, a unary architecture is obtained when $F = D$, a segmented architecture requires $D < F < N - 1$ and a binary architecture is constructed when $F = N - 1$ and $D = 0$. The previously mentioned implementations are particular cases of the proposed general algorithm, that is:

- Switching sequence post adjustment – SSPA (further A_U – unary calibrated array) [5];
- Total 3-dimensional sort-and-combine – T3D-SC (further A_S – segmented calibrated array) [10];
- Complete-Folding (further A_B – binary calibrated array) [9].

In this work, they are called “boundary algorithm cases”. For A_U algorithm case $F = D = 2$, for A_S algorithm case $F = 1$, $D = 0$ and for A_B algorithm case $F = F_{\max} = N - 1$, $D = 0$. In Fig. 4, the calibrated array for every boundary algorithm case is presented.

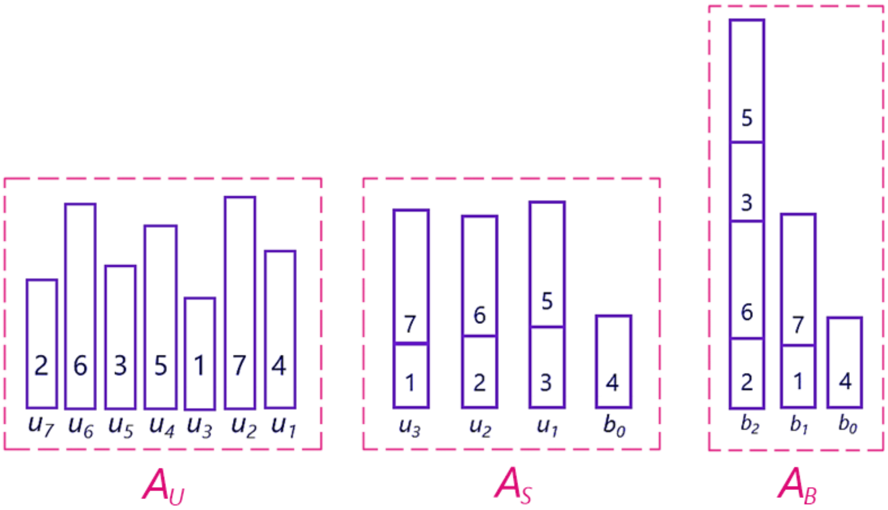

Fig. 4. Calibrated arrays for boundary algorithm cases

In order to study the efficiency of DAC static nonlinearity reduction by algorithm cases, a parametric algorithm was observed, and maximum averaged values of differential and integral nonlinearities (DNL and INL) were obtained in the research [11]. In the present work, the influence of algorithm parameters on DNL and INL exact values will be studied more thoroughly.

3. Simulation and comparison

In this section, the simulation and comparison of the results for random and systematic errors are presented. Since it is reasonable to calibrate high-resolution DACs (12 bits and more), here N resolution is 12. To perform a calibration of the primary array influenced by random errors, it is necessary to form an array of $m = 2^N$ unary elements. For each element of the primary array, a random deviation with a normal distribution is introduced. Such a normal distribution has the following parameters: mathematical expectation μ is 0 and the value of standard deviation σ is chosen to be 0.13 %. The value of σ is an example of deviation, which was derived while performing the Monte-Carlo simulation of an element (current source) for UMC 180 nm technology [12]. The number of generated primary arrays is 200. All mentioned parameters are highlighted in Table 1.

Table 1

Parameters of primary array with random errors

Resolution, N	Number of elements, m	Number of algorithm cases, M_{ex}	Mathematical expectation, μ	Standard deviation, σ	Number of arrays
12	4096	77	0	0.13 %	200

All possible algorithm cases were applied to a set of primary arrays with random deviations. As the result, transfer curves before and after calibration for each algorithm case were obtained and further used for DNL and INL calculations. In Fig. 5, the DNL and INL dependences on input code D and elements order are presented for boundary algorithm cases A_U, A_S and A_B. There is also a maximum normalized value defined for each nonlinearity dependence. As it was mentioned before, the elements

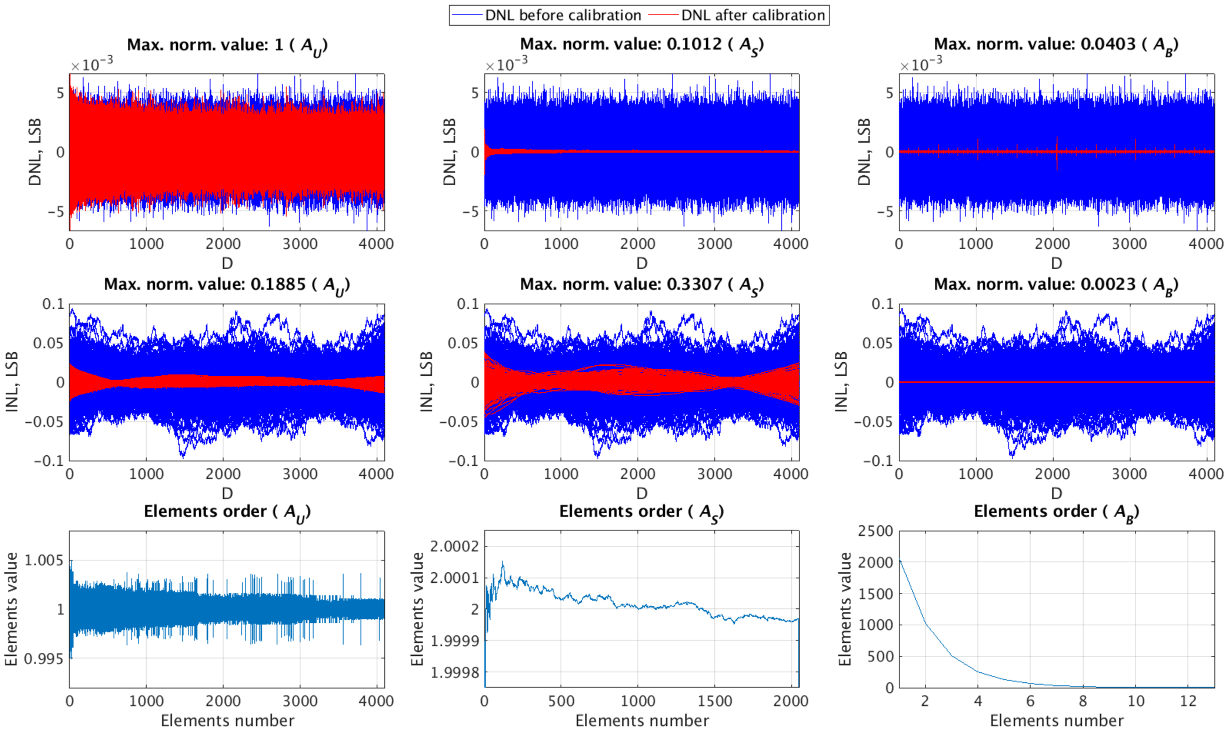

Fig. 5. Simulation results for DNL, INL and elements orders of boundary cases in presence of random errors

after application of A_U, A_S and A_B algorithm cases form unary, segmented and binary arrays respectively. The number of deviation cases illustrated in the graphs is 200.

The results show that the increment of binary segment resolution even only by one bit allows to greatly improve the DNL, which can be seen in the transition between A_U and A_S and between A_S and A_B algorithm cases. Such an improvement is possible due to presence of united elements after the folding operation. The unification reduces elements deviation and, consequently, DNL. For instance, transition from A_U to A_S reduces elements deviation and corresponding DNL by one order. However, the elements order obtained after unification deteriorated INL since element value decreases with its index. In contrast, splashes break the dependence of element value on its index in case of A_U. As a result, it leads to better INL reduction.

When comparing the obtained DNL dependences, a systematic drift of DNL can be noticed after the calibration for the A_U and A_S boundary cases, which is absent in the A_B case. To establish the reason for the systematic drift appearance, it is necessary to consider the results for DNL with fixed F from a pure unary, or unarized, array to a pure binary, or binarized, one. This will allow us to understand whether an increase in the resolution of a unary segment, or unarization, affects the appearance of a systematic drift.

In Fig. 6, the simulation results of DNL, INL and elements orders are presented. Here, algorithm cases from a bottom line of the table in Fig. 3 are considered, where $F = F_{\max} = 11$. The unarization power increases from left to right, so the leftmost case is a binarized array and the rightmost case is a unarized one. The number of deviation cases illustrated in the graphs is 200.

According to the obtained results, there is no systematic drift of DNL with an increase of unarization power. So, the unarization has no impact on the appearance of the systematic drift. Previously, the systematic drift in DNL dependences occurred for A_U and A_S algorithm cases when F was lesser than the maximum possible value $F_{\max}$. Meanwhile for A_B case, where $F = F_{\max}$, it was absent. Therefore, while studying algorithm cases with a fixed $F_{\max}$, no systematic drift was observed in the dependences.

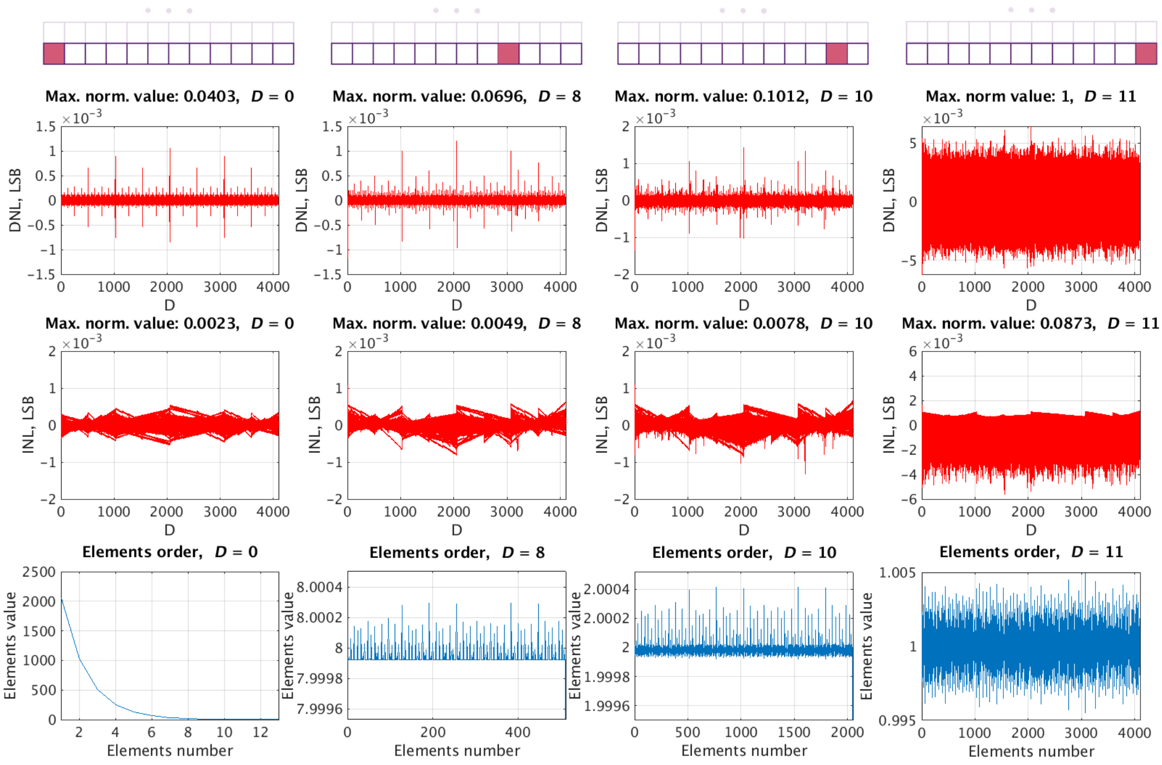

Fig. 6. Simulation results for DNL, INL and elements orders ($F = F_{\max} = 11$)

In order to establish the reason of systematic drift appearance, results of DNL, INL and elements orders for algorithm cases with different numbers of F are presented in Fig. 7. Here, algorithm cases that allow obtaining fully unarized arrays (i.e. cases on the diagonal in Fig. 3) are considered.

According to the results, the systematic drift can be seen. Moreover, with the decrement of F from the maximum possible value $F_{\max} = 11$ to the minimum possible value $F = 1$ the influence of systematic drift becomes worse. Hence, the systematic drift appears when F is lesser than the maximum possible value. Therefore, the more folding operations are done, the less is the systematic drift for DNL results in presence of random errors.

The forming of primary array influenced by systematic errors is similar to the one in presence of random errors except for the deviations introduction. A primary array of 2^N elements is formed ($N = 12$) for a further calibration. Then, according to the methodology for systematic errors forming with different profiles [13], a generation of profile parameters combinations and set of profiles systematic errors is held. Among the whole set of profiles, a joint approximation with anisotropic case is chosen to be applied to the primary array. The number of cases considered for various angles and shifts is 200.

Similarly to the case of random errors, boundary algorithm cases were applied to a primary array influenced by systematic errors. The DNL and INL were calculated using the obtained transfer curves before and after calibration. In Fig. 8, the DNL and INL dependences and elements orders are presented for boundary algorithm cases A_U, A_S and A_B.

According to the obtained results, the systematic drift, which was observed earlier for the DNL dependence in presence of random errors, provides an impact on DNL for the A_U and A_S algorithm cases in presence of systematic errors as well. However, the A_B algorithm case demonstrates the lack of systematic drift, which is also similar to the result for random errors. Therefore, the cause of such a behavior is the same for both types of errors, and one common statement can be concluded: the fewer folding operations are done, the worse is the systematic drift impact on the DNL results.

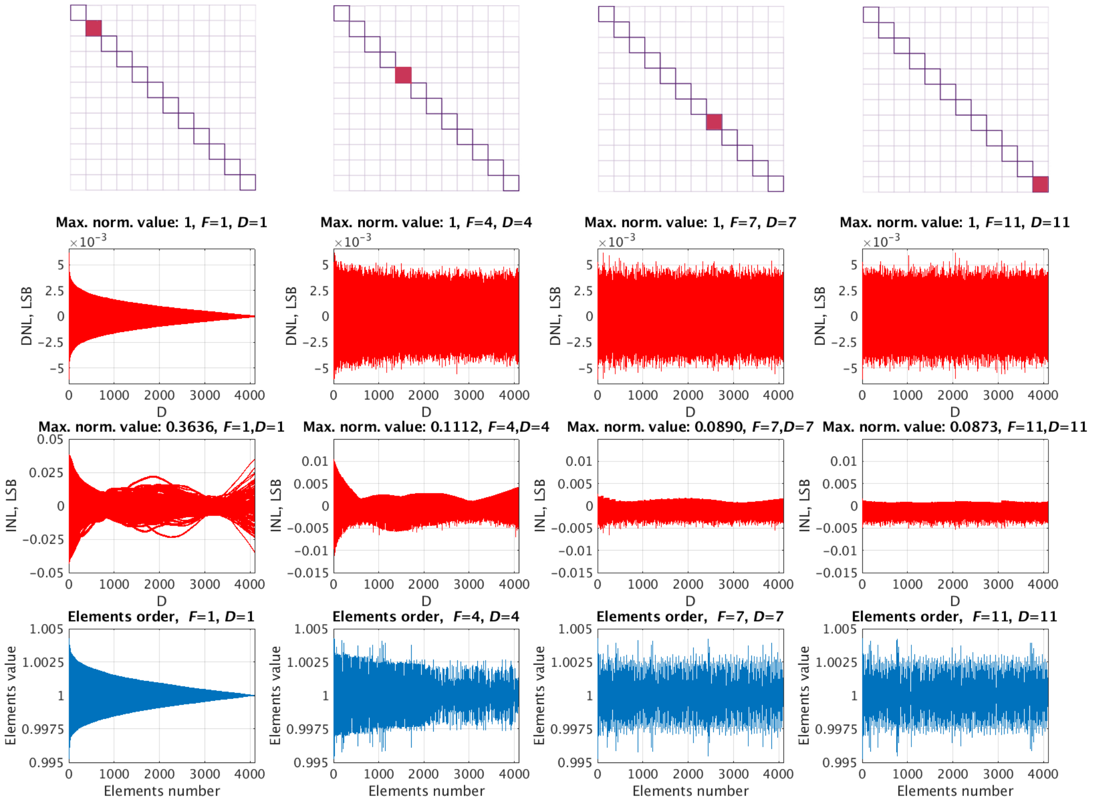

Fig. 7. Simulation results for DNL, INL and elements orders (diagonal cases)

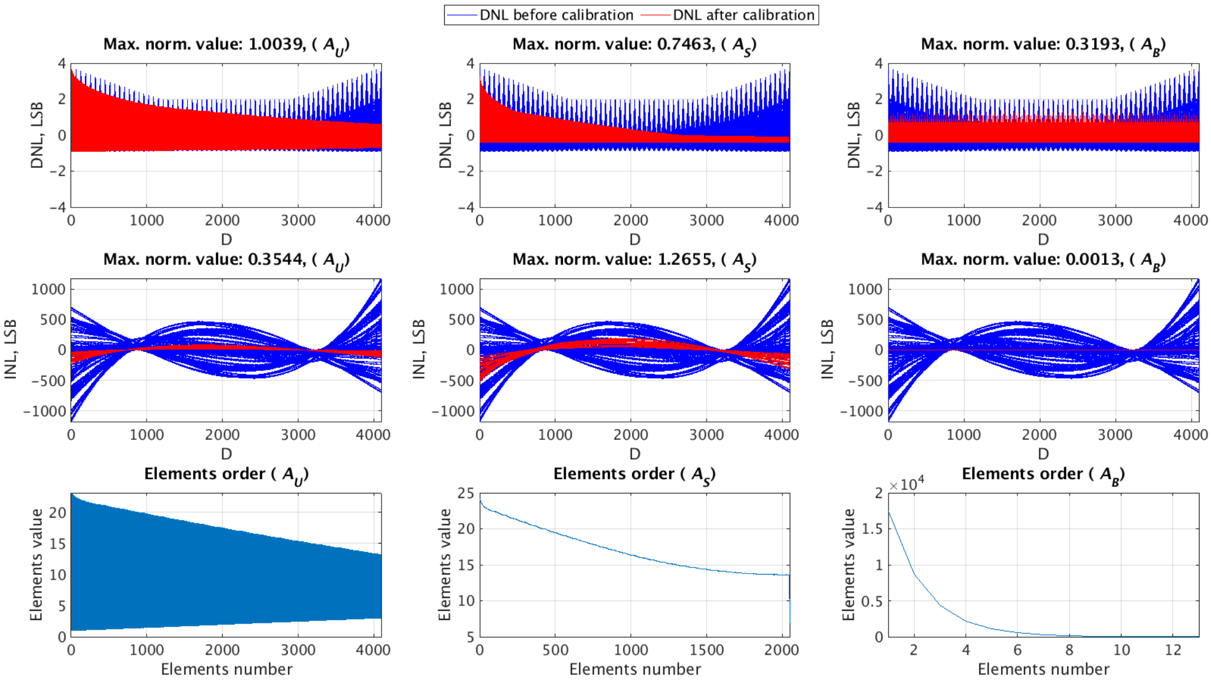

Fig. 8. Simulation results for DNL, INL and elements orders
of boundary cases in presence of systematic errors

4. Conclusion

Digital-to-analog converters (DACs) are widespread devices for converting digital data into analog signals. The linearity of conversion depends on the elements ratio, which can deviate from the nominal value during integrated circuit fabrication. To overcome this issue, a calibration is one of the possible solutions. In this work, a non-redundant switching-based calibration method is considered and the general algorithm for such a method is proposed. The intermediate implementations of the algorithm are compared by efficiency of DNL and INL reduction.

The folding and decoupling operations are introduced. One folding operation ($F = 1$) decreases the resolution of a unary segment by one bit and increases the resolution of a binary segment by one bit. One decoupling operation ($D = 1$) decreases the resolution of a binary segment by one bit and increases the resolution of a unary segment by one bit. In terms of DNL, the folding operation improves nonlinearity due to reduction of elements deviations during the elements unification. The opposite result is demonstrated by the decoupling operation, which deteriorates nonlinearity during the elements splitting. In terms of INL, the impact of folding operation depends on the elements order after calibration, which also contributes to the nonlinearity. If the elements order represents a dependence of element value on its index, then the unification has a deteriorative impact on nonlinearity in contrast to the decoupling operation, which improves it. Research [11] concluded that a simultaneous variation of both F and D does not allow definite estimation of a more efficient algorithm case in nonlinearity reduction.

All fully unarized arrays ($F = D$) provide the INL reduction, however the DNL cannot be decreased. The similar results were demonstrated in [14, 15] for the switching schemes of unary DACs. The DNL reduction can be obtained by the increment of binary segment resolution – binarization. Binarization provides an error averaging for elements, which reduces elements deviations, as they will consist of two and more parts. Such an effect is demonstrated for switching schemes with element division in [13, 14, 16]. As a result, the greater is the resolution of the binary segment, the better is the nonlinearity reduction.

The number of applied folding operations F affects the presence of systematic drift in DNL dependences for both random and systematic errors. After the sorting step of the folding operation an explicit dependence of element value on its index occurs, which has an influence on the DNL dependence in the form of the systematic drift. With the increment of F, the reordering of elements is more thorough. Thus, the greater is F, the better elements are reordered and the lesser is an explicit dependence of element value on its index. At the maximum possible number of folding operations $F_{\max}$, the array of elements is completely reordered, which results in the absence of the explicit dependence. Hence, the systematic drift in case of $F_{\max}$ is absent.

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