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SPIKING NEURAL NETWORK ANALOG TWO-VARIABLE NEURON IMPLEMENTATION

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Abstract. Currently, the problem of using neural networks in embedded systems, which have constraints on power consumption and area occupied, is relevant. At the same time, there is growing interest in spiking neural networks – more biologically realistic neural networks with potentially higher energy efficiency. This paper presents a review of existing hardware implementations of spiking neural networks, implemented both in the digital and analog domains. A hardware implementation of analog spiking neuron and synapse fabricated in Mikron JSC 180 nm CMOS technology with a reduced supply voltage of 0.6 V is presented. According to the simulation results, the energy consumption of a single neuron was 1.46 pJ/spike. The paper also provides a formula for comparing energy consumption between neurons fabricated in different technologies and with different supply voltages. According to this formula, the energy consumption of the implemented neuron is comparable to that of the referenced sources.

Keywords: spiking neural network, power consumption, spiking neuron, analog neuron, analog synapse

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РЕАЛИЗАЦИЯ АНАЛОГОВОГО ДВОИЧНОГО НЕЙРОНА ДЛЯ ИМПУЛЬСНОЙ НЕЙРОННОЙ СЕТИ

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Аннотация. В настоящее время актуальна проблема использования нейронных сетей во встраиваемых системах, в которых существуют ограничения по потребляемой мощности и занимаемой площади. В то же время растет интерес к импульсным нейронным сетям – более биологически реалистичным нейронным сетям с потенциально более высокой энергоэффективностью. В данной работе представлен обзор существующих аппаратных реализаций импульсных нейронных сетей, реализованных как в цифровой области, так и в аналоговой. Представлена аппаратная реализация аналоговых импульсных нейрона и синапса, выполненного по технологии АО «Микрон» 180 нм КМОП с пониженным напряжением питания 0,6 В. По результатам моделирования потребляемая энергия одного нейрона составила 1,46 пДж/импульс. Также в работе приведена формула для сравнения потребляемой энергии между нейронами, выполненными по разным технологиям и с разным напряжением питания. По данной формуле потребляемая энергия реализованного нейрона сопоставима со сравниваемыми источниками.

Ключевые слова: импульсная нейронная сеть, потребляемая мощность, импульсный нейрон, аналоговый нейрон, аналоговый синапс

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Introduction

Artificial neural networks (ANNs) are widely used in various areas such as classification and clustering, image and speech recognition, prediction etc. Several types of neural network are developed, for example, feed-forward neural network (FFNN), convolutional neural network (CNN), recurrent neural network (RNN) etc. ANNs can also be applied in embedded systems for vehicle driver assistance [1], real-time image recognition [2, 3], monitoring [4] etc. The use of ANNs in embedded system is limited by small area and low power consumption that leads to the need to develop specific ANNs which can meet these restrictions. Spiking neural network (SNN) uses a different type of neuron interaction compared to other ANNs. The nature of this network can be used to develop neural networks with lower power consumption that are suitable for embedded devices.

This paper describes the basics of SNNs and shows several existing approaches to spiking neuron implementations. One of the approaches has been implemented using 180 nm technology to evaluate its benefits and drawbacks.

SNN basics

Basic principle

An SNN is a next-generation of neural network that is mostly based on biological mechanisms of neuron interactions. An SNN operates with spikes – short impulses which can activate a neuron and

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Fig. 1. Spiking neuron model [5]

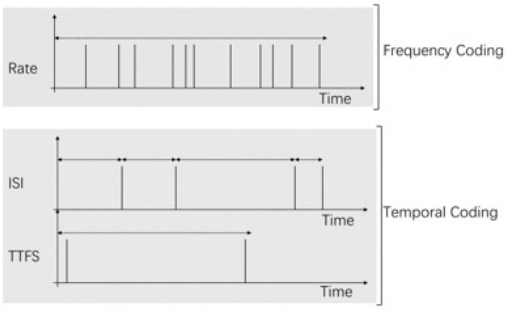


Fig. 2. Frequency and temporal encoding [5]

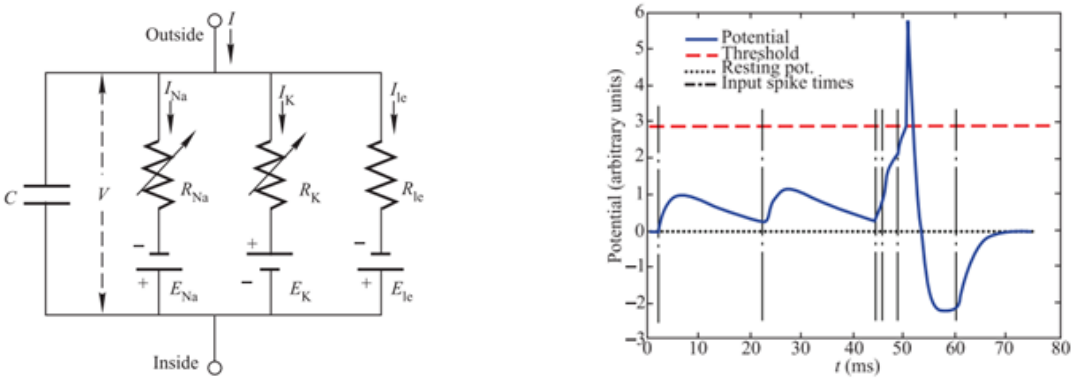


Fig. 3. Equivalent circuit and time diagram of HH model [6]

make it produce another spike. An illustrative example of a spiking neuron performance is shown in Fig. 1.

Encoding

Data encoding in SNNs is also different compared to ANNs. An SNN operates with data distributed in time, so encoding may be done by the number of spikes in a given period (frequency encoding) or by the time between spikes (temporal encoding). These types are shown in Fig. 2.

Neuron models

There are a lot of spiking neuron models. Some of them are purely mathematical models that are not applicable in hardware-implemented neural networks because of their complex computations, such as the Izhikevich model [5]. Another popular model is the Hodgkin-Huxley (HH) model [6] that includes several biological parameters of a biological neuron. The equivalent circuit and time diagram of the HH neuron model are shown in Fig. 3.

The most popular spiking neuron model is the Leaky Integrate-and-Fire (LIF) neuron [6]. In comparison with the HH model, it does not have ion potentials, but it still considers several biological mechanisms such as refractory period and leakage when there is no input excitation. All observed hardware implementations of SNN use this model of neuron due to its balance between simplicity and biological plausibility. The Integrate-and-Fire (IF) neuron model [6] does not have a refractory period and is one of the simplest spiking neuron models. However, according to a review of papers devoted to hardware implementation of neural networks, the IF model is not used as widely as the LIF one.

Hardware implementation of SNN

General device implementation

Despite focusing on hardware implementation, it is necessary to consider software-based implementations using general-purpose devices for computations such as CPUs and GPUs. In [7], a comparison between an ANN and an SNN for a classification task is presented. The data for classification were real-time ECG signals. The paper shows that the SNN accuracy was 2.5% higher than that of the ANN. However, there is no additional data in the paper to reveal which structure of ANN was used. In [8], an SNN for ECG signals processing is presented. The paper shows that the applied SNN can achieve 93–94% accuracy for real-time ECG classification.

FPGA-based implementation

FPGA is a widely used device for developing accelerators for ANN because of its high flexibility. In [9], both a new type of data encoding for SNNs and important parameters for embedded devices are presented. According to this paper, FPGA solutions in recent years can achieve 97% classification accuracy with power consumption down to 100 mW. In [10], an algorithm to switch from an ANN to an SNN to avoid the training operation for SNN is shown, which is usually more complex than training an ANN. A comparison between the starting ANN and the resulting SNN shows that the accuracy slightly decreased from 92.43 to 91.96% and power consumption decreased significantly from 0.56 to 0.20 mW.

ASIC digital implementation

When it comes to ASIC, there is a possibility to use not just a digital domain but also mixed and analog circuits to implement neural networks.

In [11], digital SNN was firstly verified using FPGA and then implemented in ASIC using 40 nm technology and a comparison of several recent papers was given. According to this comparison, the accuracy of implemented SNN achieves 90% or higher and the occupied area varies from 0.1 mm^2 to 40 mm^2. Energy consumption in the highlighted work achieve 0.75 μJ per classification. In [12], multicore coprocessor was implemented using 14 nm technology and achieves 26.7 pJ/spike energy consuming with a total occupied area 60 mm^2.

ASIC analog implementation

In [13], a full analog neuron circuit for SNN with clocked comparators is presented. This solution is implemented using 22 nm technology and achieves 87 fJ/spike energy consumption with 14000 um^2 occupied area. This work also considers a comparison between several mixed-signal approaches which shows that energy consumption can achieve values from hundreds of fJ/spike to tens of pJ/spike. In [14], an analog neuron implemented in 150 nm technology with energy consumption 55 fJ/spike and occupied area 250 um^2 is presented. It shows noticeable energy consumption but requires high-voltage additional circuits in training stage.

SNN neuron implementation

A spiking neuron and a synapse were implemented based on [15]. Their performance was then evaluated. The circuit diagram of the neuron is shown in Fig. 4.

The neuron has three units. The first unit calculates the membrane potential using a current mirror and a capacitor. The input current drives the current mirror when the input current is higher than the

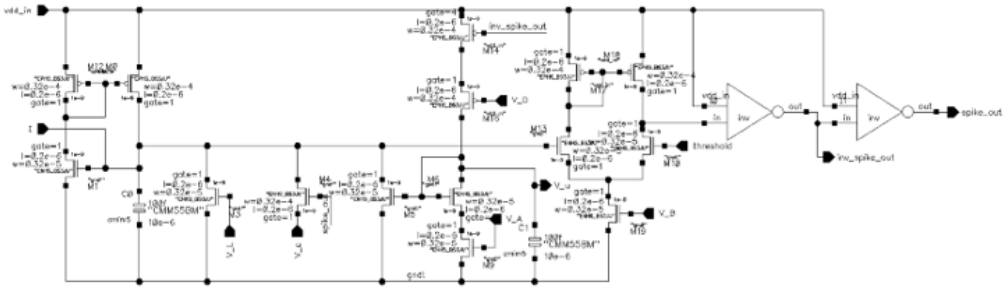


Fig. 4. Neuron circuit

leakage one. The membrane potential is proportional to the charge stored in capacitor C0 and decays through transistors M3 and M5. Transistor M5 is controlled by external voltage V_L and provides the leakage current. When a spike is generated, transistor M4 opens and the membrane potential is set to the value of external voltage V_c.

The second unit calculates the adaptation potential and its value is proportional to the charge stored in capacitor C1. When a spike is generated, transistor M14 opens and the adaptation potential is increased depending on external voltage V_D, which is the gate voltage of transistor M16. When a spike is not generated, the adaptation potential decays through transistors M6 and M9, and the latter is controlled by external voltage V_A. The current flow of transistor M5 increases as the adaptation potential increases and makes it more difficult for the membrane potential to increase.

The third unit is a comparator which is controlled by external voltages for setting the threshold and bias voltages. The circuit diagram of the synapse is shown in Fig. 5.

The neuron and the synapse were implemented using Mikron JSC 180 nm CMOS technology. The supply voltage was decreased from 1.8 V, which is standard for the technology, to 0.6 V. It allows power consumption to be reduced by moving the operating points of transistors to the sub-threshold region, as is done in the reference paper.

The simulation circuit is shown in Fig. 6.

The input source is implemented as a PMOS current mirror. The value of the input current is controlled by transistor M3 with a DC gate voltage. A pulse source is used to set the initial state. V_B voltage is set to Vdd to bring the comparator to its operating point. V_D is a PMOS gate voltage, so it is set low to let current flow when a spike is generated. V_c is a relaxation voltage, so it is also set low. V_L and V_A are set high (400 mV and 600 mV respectively) to achieve a noticeable leakage current. This simulation contains only one neuron whose output is the output of inverters, and capacitors were set as a load for it. During the simulation, the power consumption for each spike was measured, and its value is 1.46 pJ per spike.

For comparison between neurons implemented with different technologies, technology-independent energy estimation per spike is given by:

$$W = \frac{W0}{\left(\frac{T0}{T_{ref}}\right)^2 \times \left(\frac{Vdd0}{Vdd_{ref}}\right)},$$

where W is the technology-independent energy per spike, $W0$ is the technology-dependent energy per spike, $T0$ is the technology node of the evaluated circuit, T_{ref} is the reference technology node, $Vdd0$ is the voltage supply of estimated circuit and Vdd_{ref} is the reference voltage supply.

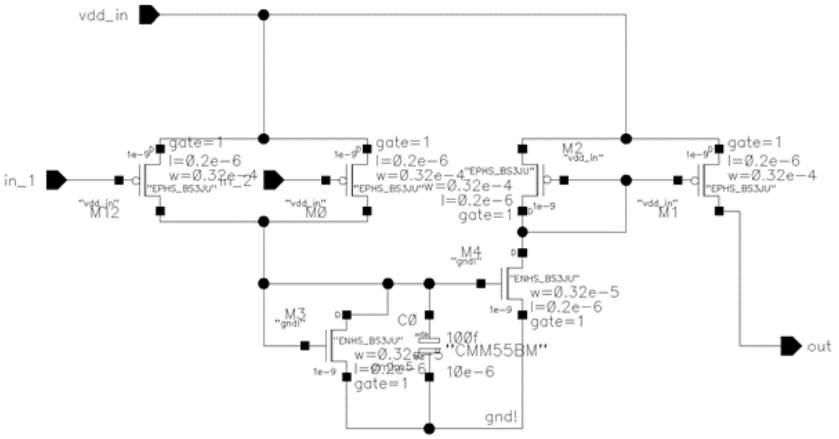


Fig. 5. Synapse circuit

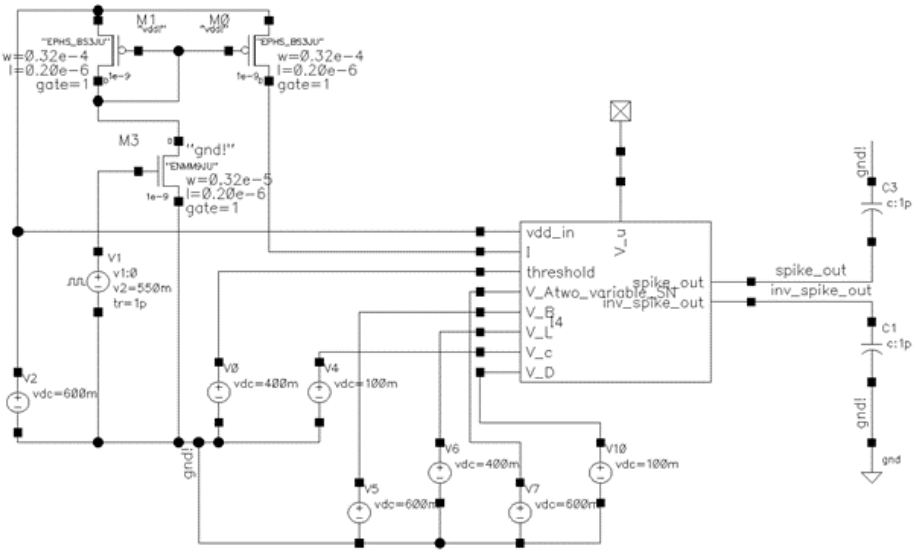


Fig. 6. Simulation circuit

According to this estimation, the neuron circuits from the references are compared with the implemented neuron circuit. Results are shown in Table 1.

Table 1

Comparison of estimated energy consumption

Neuron	Technology node	Vdd, V	Estimated W, pJ per spike
[13]	22 nm	0.8	13.06
[14]	150 nm	0.4	0.362
[15]	65 nm	0.3	4.017
This work	180 nm	0.6	4.424

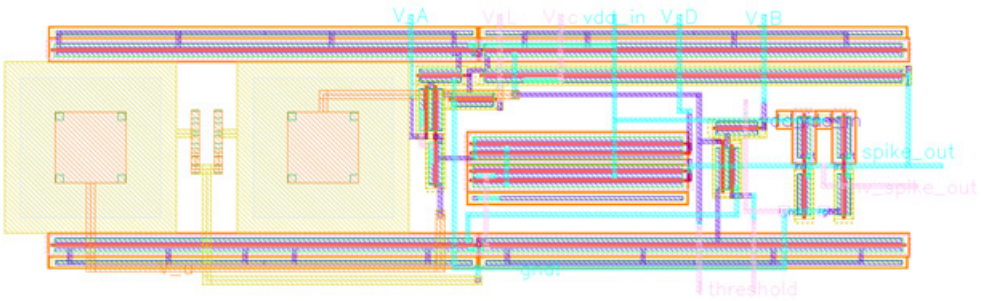


Fig. 7. SNN neuron layout

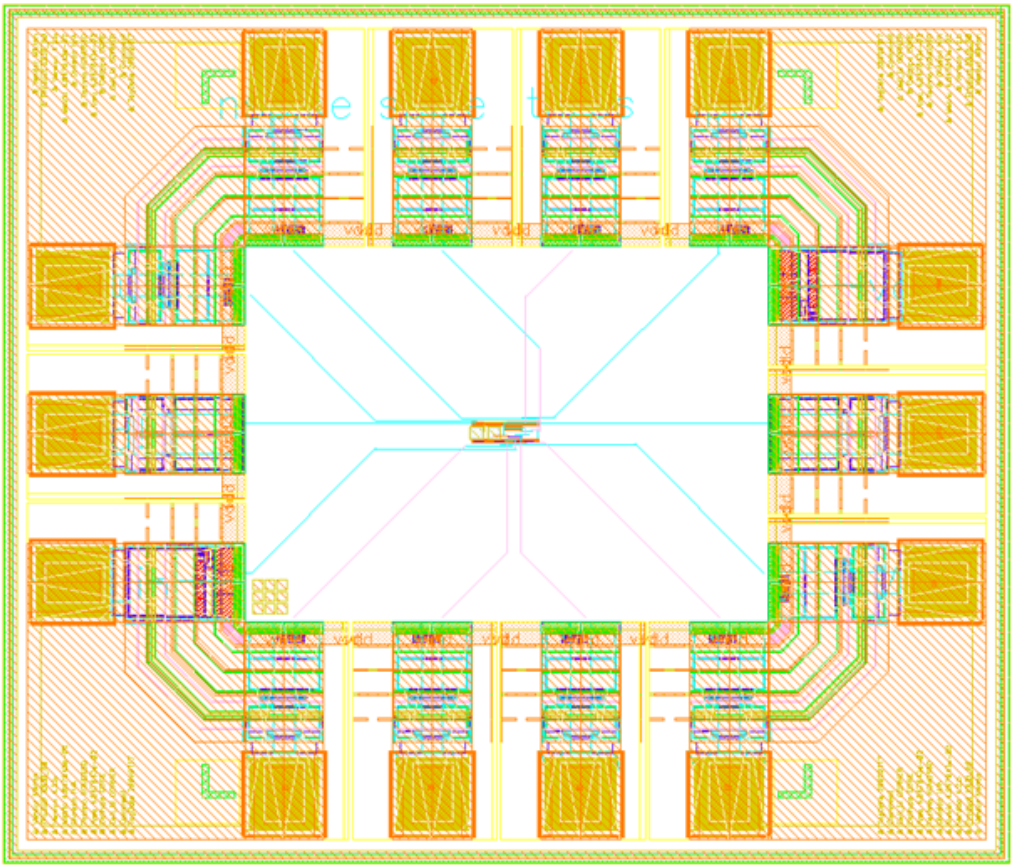


Fig. 8. Neuron with ESD guard ring

After schematic simulation, the layout of neuron circuit was designed. The layout of the SNN neuron is shown in Fig. 7. The occupied area of the neuron is 1440 μm^2. A guard ring was implemented around the chip to provide a protection against electrostatic discharge and to enable experimental measurements. The total area of the chip with the ESD guard ring is 887400 μm^2.

A synapse with two input neurons (with same weight values) and one output neuron was simulated taking into account the parasitic parameters of the SNN neuron circuit layout. A significant drawback of this synapse is that the weights of the neurons are set through the width of the transistors (M12 and M0 in Fig. 5). This will lead to weight mismatch on a real device because the effective width of the

transistors is depending on several factors of environment where this device is used and on semiconductor process effects during chip manufacturing. For further applications, it is necessary to move away from setting the weights using the transistor width and provide another method of weight setting for the SNN based on this neuron.

Conclusion

This work has presented a hardware implementation of an analog SNN neuron and a synapse with neuron energy consumption 1.46 pJ/spike at a supply voltage of 0.6 V in Mikron JSC 180 nm CMOS technology. Using the formula for comparison between implementations with different technologies, it was shown that the implementation presented in this work has comparable energy consumption compared to the reviewed works. A circuit with several neurons and their connection via a synapse was simulated to validate its performance. A drawback of the implementation presented in this work is that the neurons weights are set by the width of the synapse transistors, which will lead to weight mismatch. Further studies are required to find other ways of setting neurons weights and to reduce energy consumption of the neuron circuit for better energy efficiency.

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