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A SPIKING NEURAL NETWORK IN 180 NM CMOS

M.M. Pilipko ✉ , *D.V. Morozov*

Peter the Great St. Petersburg Polytechnic University,
St. Petersburg, Russian Federation

✉ m_m_pilipko@rambler.ru

Abstract. A hardware implementation of a spiking neural network for classifying font images of letters and numbers has been developed in the 180 nm CMOS technology of Mikron JSC. The layout dimensions are 500 × 550 μm. The supply voltage is 1.0 V. The average power consumption is approximately 0.06 mW. The clock frequency is up to 10 MHz. The neural network contains four layers of 15, 8, 8, and 10 nodes, respectively. The input data and synapse weights have a bit width of 3 bits. A comparison with the results from other studies is performed.

Keywords: CMOS, analog neural network, leaky integrating neuron

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ИМПУЛЬСНАЯ НЕЙРОННАЯ СЕТЬ ПО ТЕХНОЛОГИИ КМОП 180 НМ

М.М. Пилипко ✉ , *Д.В. Морозов*

Санкт-Петербургский политехнический университет Петра Великого,
Санкт-Петербург, Российская Федерация

✉ m_m_pilipko@rambler.ru

Аннотация. Разработана аппаратная реализация импульсной нейронной сети для классификации изображений шрифта букв и цифр в КМОП-технологии АО «Микрон» 180 нм. Размеры топологии 500 × 550 мкм. Напряжение питания 1,0 В. Средняя потребляемая мощность около 0,06 мВт. Тактовая частота до 10 МГц. Сеть содержит четыре слоя по 15, 8, 8 и 10 узлов соответственно. Входные данные и веса синапсов имеют разрядность 3 бита. Проведено сравнение с результатами других работ.

Ключевые слова: КМОП, аналоговая нейронная сеть, интегрирующий нейрон с утечкой

Финансирование: Производство интегральной микросхемы было выполнено за счет средств Министерства науки и высшего образования Российской Федерации в рамках федерального проекта «Подготовка кадров и научного фундамента для электронной промышленности» по государственному заданию «Разработка методики прототипирования электронной компонентной базы на отечественных микроэлектронных производствах на основе сервиса MPW».

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Introduction

The development of neural networks that can classify data with high speed and accuracy while consuming small power is an emerging research area. Of particular interest are spiking neural networks (SNNs), in which interactions between artificial neurons are mediated by pulses of a specific amplitude passing through functional analogs of biological junctions – synapses [1–8]. The goal of this work is to develop a four-layer analog SNN topology for classifying font images of letters and numbers, in a 5 × 3 pixel format, characterized by a small number of neural nodes and a simple neuron structure. In this paper, a hardware realization of a SNN is developed in the 180 nm CMOS technology of Mikron JSC. Simulation results taking into account the parasitic parameters of the circuit layout and pads, i.e., post-layout simulation results, are presented.

Spiking neural network

An SNN can be used in image classification. An analog neural network is potentially more efficient than a digital one. In this work, the neural network has 15 nodes in the input layer, 10 neurons in the output layer, and also has two hidden layers with 8 neurons each (Fig. 1, *a*).

Fig. 1*b* shows the main blocks of the SNN chip. The chip consists of: input data register, control circuit, spike generators, synapse register, first and second hidden layers, output layer, and counters with output register. The input data, as well as the synapse weights, are fed to a register in parallel form. The input layer generates spikes, whose number is proportional to the input value. Synapses transmit these spikes to neurons in the next layer. The neuron's capacitor is charged by the spikes,

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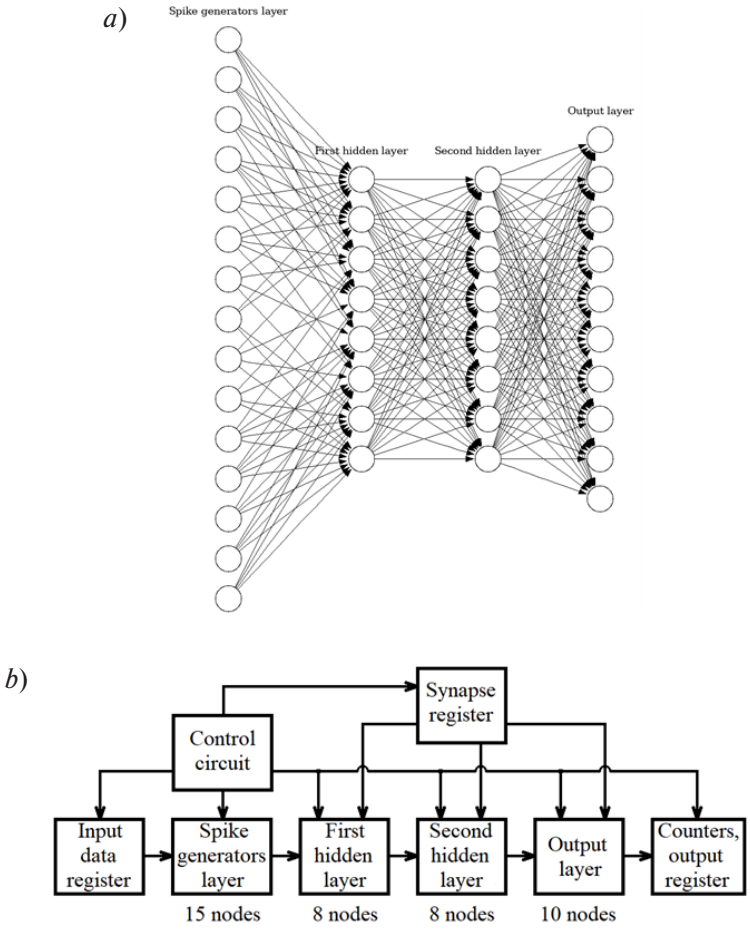


Fig. 1. SNN

with the current proportional to the synapse weight. When a threshold is exceeded, the neuron generates ("fires") its own spike, which is passed on to the next layer, while the capacitor is reset. Neurons are implemented using the leaky integrate-and-fire (LIF) neuron model. Spikes from neurons in the output layer are counted by counters. The counter codes are the network's output signal. The decision corresponds to the node that has produced the maximum code. The input data and the synapse weights have a 3-bit resolution. Silence mode, synapse weights setting mode, data input/output mode, and operating mode are supported. The working cycle including input data writing, network operation, and data output, takes 36 clock periods. Default synapse weights and default input data can be set for control. The comparator thresholds in each internal layer and in the output layer can be controlled. The neuron charge leakage rate can be adjusted. The output of one of the neurons is routed from each layer to control spike generation.

Examples of the synapse circuit are presented in [2, 6–8]. The synapse circuit designed in this work is shown in Fig. 2, *a*. In accordance with Fig. 1, the input of each neuron is connected to eight synapses. The spike "SPK" is transmitted via the synapse. The weight of the synapse is set using the values "W<0:2>" that are stored in a row of synapse register (Fig. 1, *b*). The output node "MEM" is used to connect neuron capacitor. The data "D<0:2>" on MOSFETs' gates of single-finger M1, two-finger M2, and four-finger M3 determines charge current of the neuron capacitor.

The neuron circuit designed in this work is shown in Fig. 2, *b*. The circuit consists of three parts: comparator on MOSFETs M1–M11; analog memory element on MOSFETs M12–M16, neuron capacitor C1, and inverter I9; and logic part I1–I8. The signal "LEAK" sets the rate of charge leakage

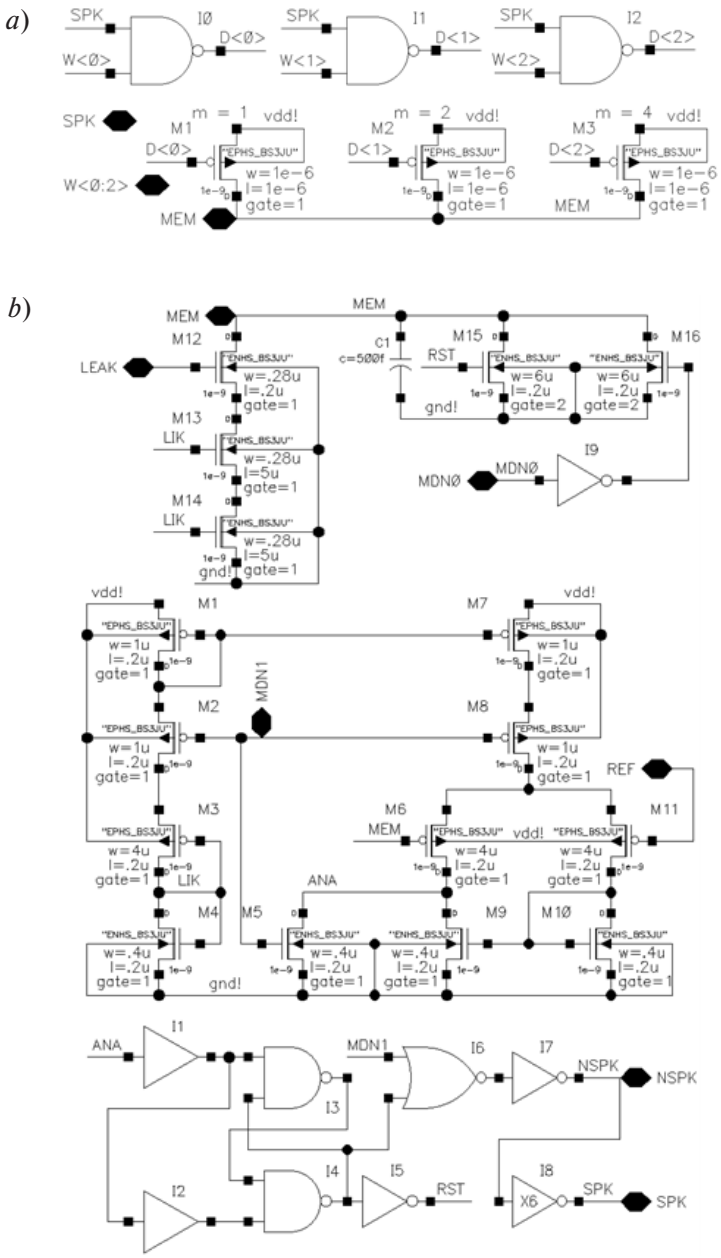


Fig. 2. Synapse and neuron circuits

of the neuron capacitor. The signal “MDN1” enables the comparator operation during operating mode of the SNN and disables the comparator in other modes. The comparator compares the signals “REF” and “MEM”, generates its output signal “ANA”, which is the input signal to the logic. Buffer I1 consists of four series-connected identical CMOS inverters. Buffer I2 consists of six series-connected CMOS inverters with different transistor lengths and defines the pulse width of the output spike. The NANDs I3 and I4 form an SR latch, while CMOS inverter I5 produces reset signal “RST” for discharging the neuron capacitor C1. The signal “MDN0” enables the discharge of the neuron capacitor C1 in silence mode. The signal “SPK” is the neuron’s output, while the signal “NSPK” provides the ability to control data in layers of the SNN using measuring equipment. The CMOS inverter I8 uses six-finger MOSFETs to increase neuron’s load capacity. The signal “LIK”, formed in the comparator, is an additional biasing signal for analog memory element.

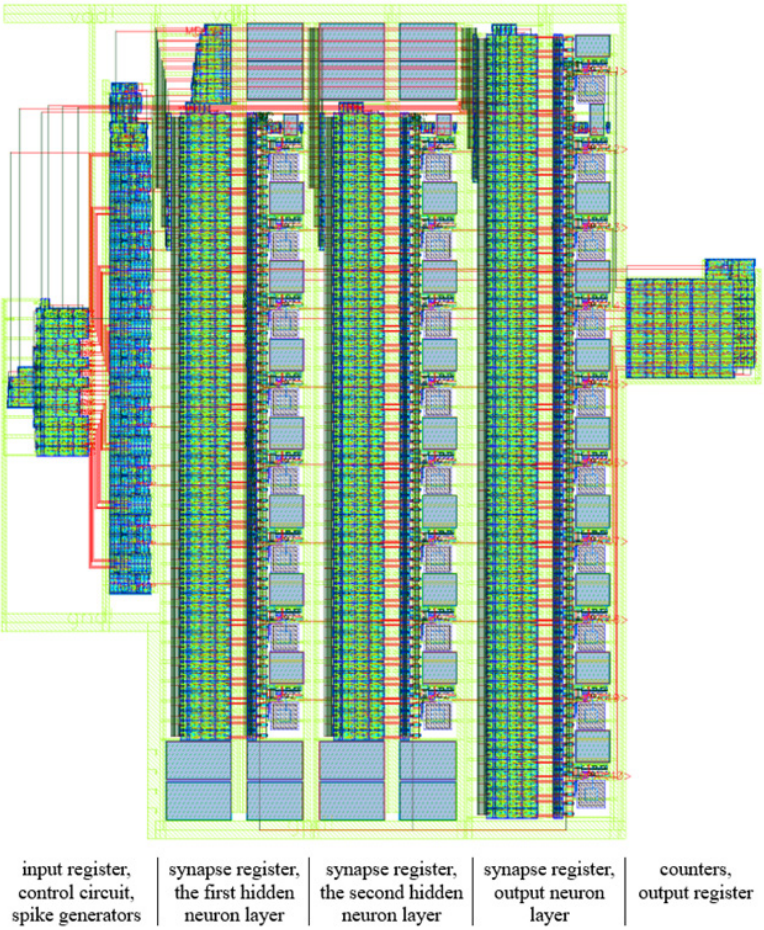


Fig. 3. SNN circuit layout

The layout of the SNN circuit is shown in Fig. 3 and has dimensions 500 × 550 μm. The layout consists of columns representing some main parts, namely input data register, control circuit and spike generators, synapse registers, neurons of the first and second hidden layers, neurons of the output layer, and counters with the output register in accordance with Fig. 1, *b*.

The supply voltage of Mikron JSC 180 nm CMOS technology is 1.8 V, but at this voltage the SNN circuit has high-power consumption, ca. 0.5 mW. It is possible to decrease power consumption by using supply voltage of 1.0 V. At this voltage the SNN circuit still works correctly while consuming only 0.06 mW.

Fig. 4 shows the operation of a neuron. The signal "CLK" represents the input spikes from previous neural network layer. The reference level "REF" is equal to 250 mV (dot-dashed line). There are two signals of neuron memory shown at different leakage control voltages that are equal to 0.1 V and 1.0 V. For "MEM_0.1" (dashed line), the leakage of the neuron is less than for "MEM_1.0" (continuous line). If the reference level is exceeded by the value in the neuron's memory, a spike "SPK" is formed.

Fig. 5 shows the process of writing the input data into 15 neurons of the SNN input layer as well as generation of spikes as a results of post-layout simulation. Signals "MODE<1>" and "MODE<2>" define SNN working mode, at MODE<1> = 0 and MODE<2> = 1, the input data writing is performed. The input data has a 3-bit resolution and is shown in Fig. 5 in decimal representation as "CODE" from 0 to 7. The input data writing is performed at a fall of the signal pulse "CLK<2>". At MODE<1> = = 0 and MODE<2> = 0, the neural network is in silence mode. The outputs of spike generators in input layer are indicated from "SP_1<1>" to "SP_1<15>". In operating mode at MODE<1> = 1 and

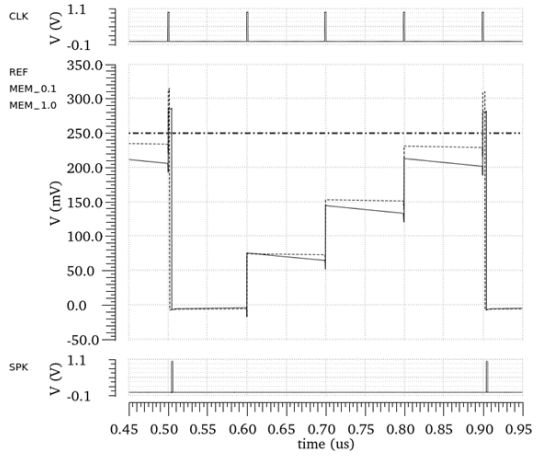


Fig. 4. Neuron operation

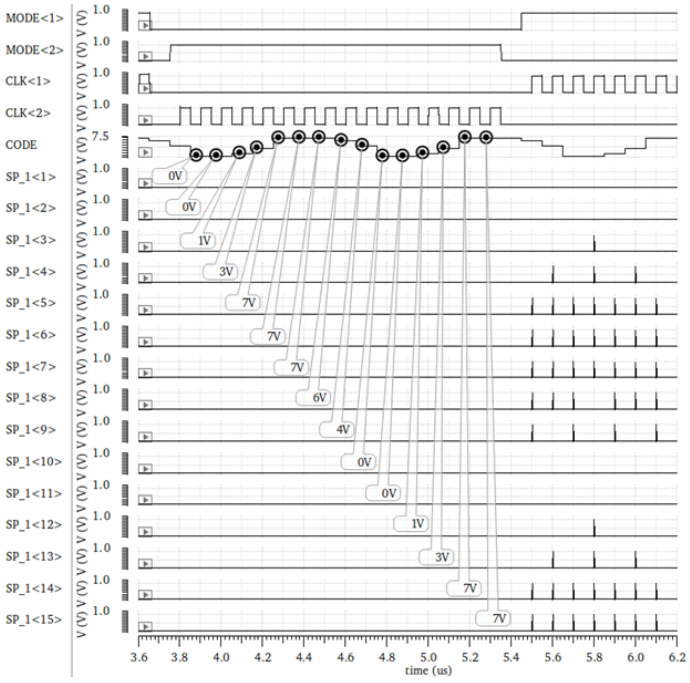


Fig. 5. The input data writing and spikes generation

MODE<2> = 0, the input layer generates spikes (their number can vary from 0 to 7) at the rise of the signal pulse “CLK<1>”. The number of spikes is equal to the input value of “CODE”. Synapses transmit these spikes to neurons in the next layer.

Fig. 6, *a* shows spikes generation in four layers of the neural network as the results of post-layout simulation. As seen, in operating mode at MODE<1> = 1 and MODE<2> = 0, the input layer generates six spikes on “SP_1<1>”, the first hidden layer – three spikes on “SP_2<1>”, the second hidden layer – two spikes on “SP_3<1>”, and the output layer – two spikes on “SP_4<1>”. To check the data in SNN layers using standard measuring equipment, signals “SP_1_pulse”, “SP_2_pulse”, “SP_3_pulse”, and “SP_4_pulse” are formed and have detectable pulse durations ca. 0.05 μs similar to that of “CLK<1>”.

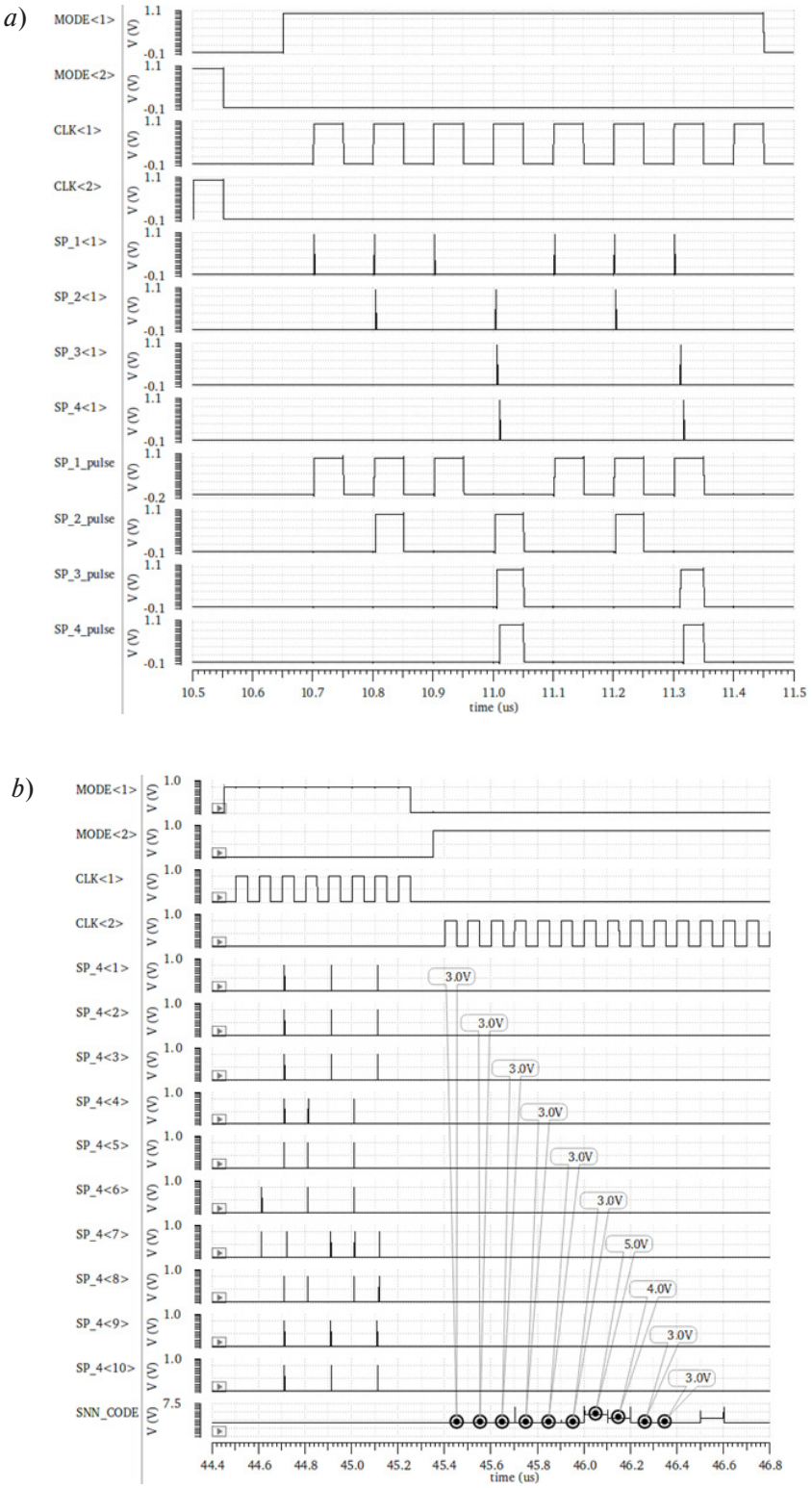


Fig. 6. Spikes generation in four layers and SNN result output

Fig. 6*b* shows the process of reading the output data out of 10 neurons of the SNN output layer as the results of post-layout simulation. The spikes of the output layer are indicated from "SP_4<1>" to "SP_4<10>". In operating mode at MODE<1> = 1 and MODE<2> = 0, the output layer generates spikes from 0 to 7 at the rise of the signal pulse "CLK<1>". At MODE<1> = 0 and MODE<2> = 0,

the neural network is in silence mode. The output data reading is performed at MODE<1> = 0 and MODE<2> = 1. The output data has a 3-bit resolution and is shown in Fig. 6*b* in decimal representation as "SNN_CODE", i.e., the values can be from 0 to 7. The output data reading is performed at the fall of the signal pulse "CLK<2>". As seen, the value of "SNN_CODE" is proportional to the number of spikes.

Main characteristics of the realized SNN are summarized in Table 1 in comparison with the results published in [2]. Complexity/Area and Complexity/Power are near to those in [2].

Table 1

Comparison of results

Main characteristics	This work	[2]
CMOS technology	180 nm	180 nm
Architecture	Analog	Analog
Classifier type	SNN	SNN
Neuron Model	LIF	LIF
Area	0.275 mm^2	3.6 mm^2
Power consumption	0.06 mW	1.06 mW
Complexity [Total number of weights]	208	3311
Complexity/Area	756	920
Complexity/Power	3467	3123

Conclusion

The hardware realization of the SNN in the 180 nm CMOS technology of Mikron JSC has been discussed. In comparison with the results published in [2], this work provides competitive values of Complexity/Area and Complexity/Power characteristics.

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INFORMATION ABOUT AUTHORS / СВЕДЕНИЯ ОБ АВТОРАХ

Mikhail M. Pilipko
Пилипко Михаил Михайлович
E-mail: m_m_pilipko@rambler.ru
ORCID: https://orcid.org/0000-0003-3813-6846

Dmitry V. Morozov
Морозов Дмитрий Валерьевич
E-mail: dvmorozov@inbox.ru
ORCID: https://orcid.org/0000-0003-3403-0120

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